********** FLIP-FLOP TIMING INFO **********

2u SPECIAL FLIP FLOP TIMING

Data Setup time = 5.50 ns.

Data Hold time = 7.50 ns.

Maximum clock rise time

Clock pulse width = 8.50 ns.

Reset pulse width = 8.00 ns.

Set pulse width = 9.50 ns.

3u SPECIAL FLIP FLOP TIMING

Data Setup time = 10.50 ns.

Data Hold time = 9.50 ns.

Maximum clock rise time

Clock pulse width = 13.50 ns.

Reset pulse width = 12.50 ns.

Set pulse width = 13.50 ns.

********** SPICE DECK CONTINUED **********

```
M88x8 23 55 153 gnd NMOS W=18.0U L=2.0U
M92x8 153 32 gnd gnd NMOS W=18.0U L=2.0U
M110x8 gnd 23 154 gnd NMOS W=11.0U L=2.0U
M114x8 154 21 33 gnd NMOS W=11.0U L=2.0U
M122x8 33 36 Q_b gnd NMOS W=19.0U L=2.0U
M130x5 Q_b 22 155 gnd NMOS W=22.0U L=2.0U
M137x4 155 31 gnd gnd NMOS W=14.0U L=2.0U
M156x4 gnd 33 156 gnd NMOS W=23.0U L=2.0U
M160x4 156 32 31 gnd NMOS W=23.0U L=2.0U
```

# Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

| SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY | **dfbf311** D_FF_W/SET_&_RESET | DATE: Mar 11,1989 VERSION: dlmV2.0 |
|---|---|---|

********** SPICE DECK **********

*** Generated from dfbf311.mag by magic's spice generator
*** technology: scmos
*** timestamp: 604100040
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M8x46 36 21 vdd vdd PMOS W=24.0U L=2.0U
M16x46 vdd 64 21 vdd PMOS W=24.0U L=2.0U
M36x38 vdd 20 120 vdd PMOS W=32.0U L=2.0U
M40x38 120 21 55 vdd PMOS W=32.0U L=2.0U
M50x49 55 36 122 vdd PMOS W=21.0U L=2.0U
M8x4 36 21 gnd gnd NMOS W=18.0U L=2.0U
M16x4 gnd 64 21 gnd NMOS W=18.0U L=2.0U
M50x34 55 36 121 vdd PMOS W=11.0U L=2.0U
M54x34 121 23 vdd vdd PMOS W=11.0U L=2.0U
M68x35 122 22 vdd vdd PMOS W=35.0U L=2.0U
M84x46 vdd 55 23 vdd PMOS W=24.0U L=2.0U
M92x46 23 32 vdd vdd PMOS W=23.0U L=2.0U
M100x46 vdd 23 123 vdd PMOS W=20.0U L=2.0U
M105x46 123 36 33 vdd PMOS W=20.0U L=2.0U
M113x39 33 21 Q_b vdd PMOS W=27.0U L=2.0U
M121x39 Q_b 22 vdd vdd PMOS W=27.0U L=2.0U
M133x39 vdd 31 Q_b vdd PMOS W=27.0U L=2.0U
M148x37 31 33 vdd vdd PMOS W=29.0U L=2.0U
M160x39 vdd 32 31 vdd PMOS W=27.0U L=2.0U
M34x4 gnd 20 150 gnd NMOS W=17.0U L=2.0U
M38x4 150 36 55 gnd NMOS W=17.0U L=2.0U
M46x4 55 21 151 gnd NMOS W=17.0U L=2.0U
M56x4 151 23 152 gnd NMOS W=11.0U L=2.0U
M64x5 152 22 gnd gnd NMOS W=19.0U L=2.0U

3-micron delay information.

| Path | Timing | Nominal Case | | Worst Case | |
|---|---|---|---|---|---|
| | | No Load | 1pF | No Load | 1pF |
| CLK2---Q | Pd 0--1 | 10.00 | 12.15 | 15.77 | 19.07 |
| | Pd 1--0 | 11.04 | 13.09 | 17.78 | 20.73 |
| | Tr 0--1 | 4.80 | 9.26 | 5.89 | 12.20 |
| | Tf 1--0 | 4.11 | 7.33 | 4.70 | 10.46 |
| SET4---Q | Pd 0--1 | 3.72 | 6.01 | 6.59 | 11.27 |
| | Pd 1--0 | N/A | N/A | N/A | N/A |
| | Tr 0--1 | 6.05 | 8.21 | 11.57 | 14.49 |
| | Tf 1--0 | N/A | N/A | N/A | N/A |
| RST3---Q | Pd 0--1 | N/A | N/A | N/A | N/A |
| | Pd 1--0 | 14.79 | 16.84 | 22.19 | 25.54 |
| | Tr 0--1 | N/A | N/A | N/A | N/A |
| | Tf 1--0 | 4.84 | 7.54 | 5.23 | 10.08 |
| CLK2---Q_b | Pd 0--1 | 13.41 | 18.54 | 20.81 | 27.70 |
| | Pd 1--0 | 12.15 | 17.41 | 18.99 | 26.88 |
| | Tr 0--1 | 4.11 | 9.78 | 4.82 | 13.24 |
| | Tf 1--0 | 3.42 | 9.15 | 5.38 | 12.18 |
| SET4---Q_b | Pd 0--1 | N/A | N/A | N/A | N/A |
| | Pd 1--0 | 5.77 | 10.65 | 10.24 | 18.72 |
| | Tr 0--1 | N/A | N/A | N/A | N/A |
| | Tf 1--0 | 3.87 | 8.52 | 5.49 | 12.14 |
| RST3---Q_b | Pd 0--1 | 3.27 | 5.88 | 5.73 | 11.09 |
| | Pd 1--0 | N/A | N/A | N/A | N/A |
| | Tr 0--1 | 5.74 | 10.33 | 11.57 | 17.85 |
| | Tf 1--0 | N/A | N/A | N/A | N/A |

2-micron delay information.

| Path | Timing | Nominal Case | | Worst Case | |
|---|---|---|---|---|---|
| | | No Load | 1pF | No Load | 1pF |
| CLK2---Q | Pd 0--1 | 3.14 | 4.76 | 6.91 | 10.47 |
| | Pd 1--0 | 3.32 | 4.70 | 7.30 | 10.34 |
| | Tr 0--1 | 1.39 | 4.71 | 3.06 | 10.36 |
| | Tf 1--0 | 1.20 | 3.63 | 2.64 | 7.99 |
| SET4---Q | Pd 0--1 | 1.32 | 2.74 | 2.90 | 6.03 |
| | Pd 1--0 | N/A | N/A | N/A | N/A |
| | Tr 0--1 | 2.60 | 3.58 | 5.72 | 7.88 |
| | Tf 1--0 | N/A | N/A | N/A | N/A |
| RST3---Q | Pd 0--1 | N/A | N/A | N/A | N/A |
| | Pd 1--0 | 4.49 | 5.46 | 9.88 | 12.01 |
| | Tr 0--1 | N/A | N/A | N/A | N/A |
| | Tf 1--0 | 1.20 | 3.70 | 2.64 | 8.14 |
| CLK2---Q_b | Pd 0--1 | 3.94 | 7.68 | 8.67 | 16.90 |
| | Pd 1--0 | 3.72 | 7.65 | 8.18 | 16.83 |
| | Tr 0--1 | 1.22 | 5.28 | 2.68 | 11.62 |
| | Tf 1--0 | 0.98 | 5.10 | 2.16 | 11.22 |
| SET4---Q_b | Pd 0--1 | N/A | N/A | N/A | N/A |
| | Pd 1--0 | 1.79 | 5.16 | 3.94 | 11.35 |
| | Tr 0--1 | N/A | N/A | N/A | N/A |
| | Tf 1--0 | 1.31 | 4.70 | 2.88 | 10.34 |
| RST3---Q_b | Pd 0--1 | 1.00 | 3.17 | 2.20 | 6.97 |
| | Pd 1--0 | N/A | N/A | N/A | N/A |
| | Tr 0--1 | 2.55 | 5.30 | 5.61 | 11.66 |
| | Tf 1--0 | N/A | N/A | N/A | N/A |

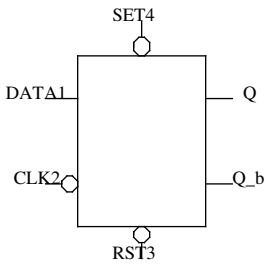
Cell Device Sizes

| Transistor | Width (λ) | Length (λ) |
|---|---|---|
| 61 | 14 | 2 |
| 52 | 19 | 2 |
| 60 | 22 | 2 |
| 57 | 11 | 2 |
| 53 | 11 | 2 |
| 54 | 17 | 2 |
| 51 | 17 | 2 |
| 50 | 17 | 2 |
| 64 | 18 | 2 |
| 65 | 18 | 2 |
| 56 | 18 | 2 |
| 55 | 18 | 2 |
| 58 | 11 | 2 |
| 59 | 19 | 2 |
| 63 | 23 | 2 |
| 62 | 23 | 2 |
| 29 | 27 | 2 |
| 31 | 27 | 2 |
| 30 | 27 | 2 |
| 28 | 20 | 2 |
| 25 | 24 | 2 |
| 27 | 20 | 2 |
| 26 | 23 | 2 |
| 34 | 24 | 2 |
| 35 | 24 | 2 |
| 21 | 32 | 2 |
| 20 | 32 | 2 |
| 33 | 29 | 2 |
| 32 | 27 | 2 |
| 24 | 11 | 2 |
| 23 | 11 | 2 |
| 22 | 35 | 2 |
| 36 | 21 | 2 |

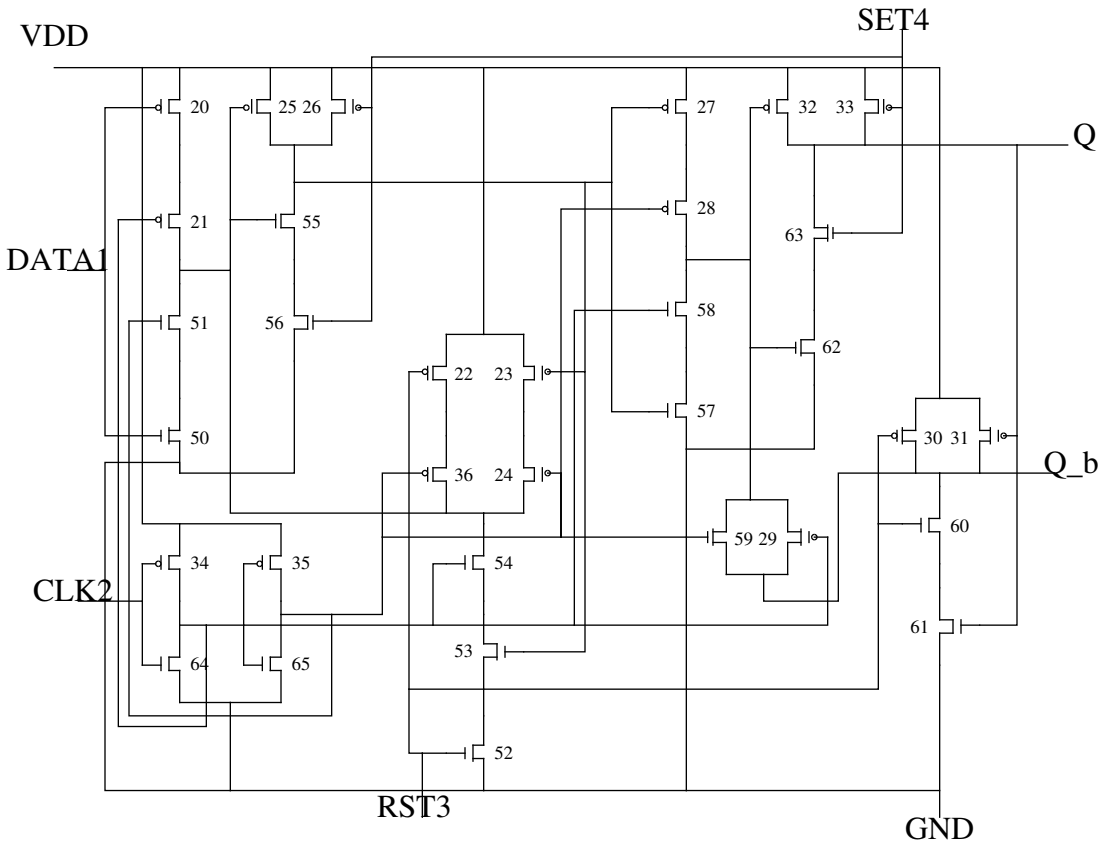
# Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

| SCALABLE CMOS (SCMOS)<br>DOUBLE METAL I / C<br>STANDARD CELL LIBRARY | **dfbf311**<br>D_FF_W/SET_&_RESET | DATE: Mar 11,1989<br>VERSION: dlmV2.0 |
|---|---|---|




SYMBOL



LOGIC EQUATIONS: Qn = {[(Qn-1*C)+(Dn-1*C)]*R}+S'
Qn'=(.NOT.Qn)+R"

Truth Table

| C | D | R | S | Q | Q' |
|---|---|---|---|---|---|
| l2h | - | 1 | 1 | Qn-1 | Qn-1' |
| h2l | - | 1 | 1 | Dn-1 | Dn-1' |
| - | - | 0 | 1 | 0 | 1 |
| - | - | 1 | 0 | 1 | 0 |
| - | - | 0 | 0 | 1 | 1 |
| - | - | - | 0 | 1 | - |
| - | - | 0 | - | - | 1 |

# Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

| SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY | **dfbf311** D_FF_W/SET_&_RESET | DATE: Mar 11,1989 VERSION: dlmV2.0 |
|---|---|---|

TERMINAL LOCATION (In Lambda)

| GRID | PIN_NAME | Y_LOC | CLASS |
|---|---|---|---|
| 1 | FeedThru | ---- | ---- |
| 2 | FeedThru | ---- | ---- |
| 3 | CLK2 | 29 | 1 |
| 4 | DATA1 | 29 | 0 |
| 5 | FeedThru | ---- | ---- |
| 6 | Blocked | | ---- |
| 7 | Blocked | | ---- |
| 8 | FeedThru | ---- | ---- |
| 9 | FeedThru | ---- | ---- |
| 10 | RST3 | 29 | 3 |
| 11 | SET4 | 29 | 2 |
| 12 | FeedThru | ---- | ---- |
| 13 | FeedThru | ---- | ---- |
| 14 | FeedThru | ---- | ---- |
| 15 | FeedThru | ---- | ---- |
| 16 | FeedThru | ---- | ---- |
| 17 | FeedThru | ---- | ---- |
| 18 | Q_b | 23 | 0 |
| 19 | FeedThru | ---- | ---- |
| 20 | FeedThru | ---- | ---- |
| 21 | Q | 30 | 0 |