********** FLIP-FLOP TIMING INFO **********

2u SPECIAL FLIP FLOP TIMING

Data Setup time = 7.00 ns.

Data Hold time = 6.00 ns.

Maximum clock rise time

Clock pulse width = 8.00 ns.

3u SPECIAL FLIP FLOP TIMING

Data Setup time = 11.50 ns.

Data Hold time = 7.50 ns.

Maximum clock rise time

Clock pulse width = 12.50 ns.

********** SPICE DECK CONTINUED **********

```
M104x11 gnd Q_b 61 gnd NMOS W=13.0U L=2.0U
M112x11 61 Q_b gnd gnd NMOS W=13.0U L=2.0U
```

********** SPICE DECK **********

*** Generated from dfnf311.mag by magic's spice generator
*** technology: scmos
*** timestamp: 605470862
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M8x39 53 CLK2 vdd vdd PMOS W=31.0U L=2.0U
M24x39 vdd 53 57 vdd PMOS W=31.0U L=2.0U
M40x47 60 22 vdd vdd PMOS W=21.0U L=2.0U
M48x47 vdd 21 120 vdd PMOS W=23.0U L=2.0U
M52x47 120 53 22 vdd PMOS W=23.0U L=2.0U
M8x4 53 CLK2 gnd gnd NMOS W=22.0U L=2.0U
M24x4 gnd 53 57 gnd NMOS W=22.0U L=2.0U
M64x44 22 60 121 vdd PMOS W=14.0U L=2.0U
M68x44 121 57 vdd vdd PMOS W=14.0U L=2.0U
M80x41 vdd 57 122 vdd PMOS W=25.0U L=2.0U
M84x41 122 60 Q_b vdd PMOS W=25.0U L=2.0U
M92x44 Q_b 53 123 vdd PMOS W=13.0U L=2.0U
M96x44 123 61 vdd vdd PMOS W=13.0U L=2.0U
M104x44 vdd Q_b 61 vdd PMOS W=26.0U L=2.0U
M112x44 61 Q_b vdd vdd PMOS W=26.0U L=2.0U
M40x4 60 22 gnd gnd NMOS W=19.0U L=2.0U
M48x4 gnd 57 150 gnd NMOS W=19.0U L=2.0U
M52x4 150 21 22 gnd NMOS W=19.0U L=2.0U
M64x15 22 60 151 gnd NMOS W=9.0U L=2.0U
M68x15 151 53 gnd gnd NMOS W=9.0U L=2.0U
M80x14 gnd 53 152 gnd NMOS W=8.0U L=2.0U
M84x14 152 60 Q_b gnd NMOS W=8.0U L=2.0U
M92x15 Q_b 57 153 gnd NMOS W=9.0U L=2.0U
M96x15 153 61 gnd gnd NMOS W=9.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
CLK2---Q	Pd 0--1	3.82	9.62	8.40	21.16
	Pd 1--0	4.07	9.06	8.95	19.93
	Tr 0--1	1.19	5.03	2.62	11.07
	Tf 1--0	1.02	4.39	2.24	9.66
CLK2---Q_b	Pd 0--1	3.70	7.03	8.14	15.47
	Pd 1--0	3.27	6.90	7.19	15.18
	Tr 0--1	3.32	10.95	7.30	24.09
	Tf 1--0	3.47	11.01	7.63	24.22

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
CLK2---Q	Pd 0--1	9.58	17.57	15.81	27.53
	Pd 1--0	10.49	17.27	16.85	26.38
	Tr 0--1	3.36	8.81	3.87	11.33
	Tf 1--0	3.10	7.56	3.46	9.79
CLK2---Q_b	Pd 0--1	9.38	14.01	14.87	20.93
	Pd 1--0	7.86	12.64	13.67	21.21
	Tr 0--1	8.76	20.20	11.21	25.97
	Tf 1--0	8.40	18.65	11.73	25.50

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
52	19	2
51	19	2
50	19	2
56	26	2
55	8	2
54	8	2
58	22	2
59	22	2
53	9	2
60	9	2
61	9	2
57	9	2
22	21	2
21	23	2
20	23	2
23	14	2
30	14	2
26	52	2
31	13	2
27	13	2
28	31	2
29	31	2
25	25	2
24	25	2

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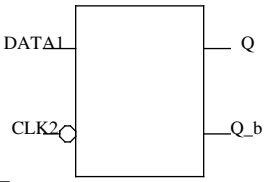
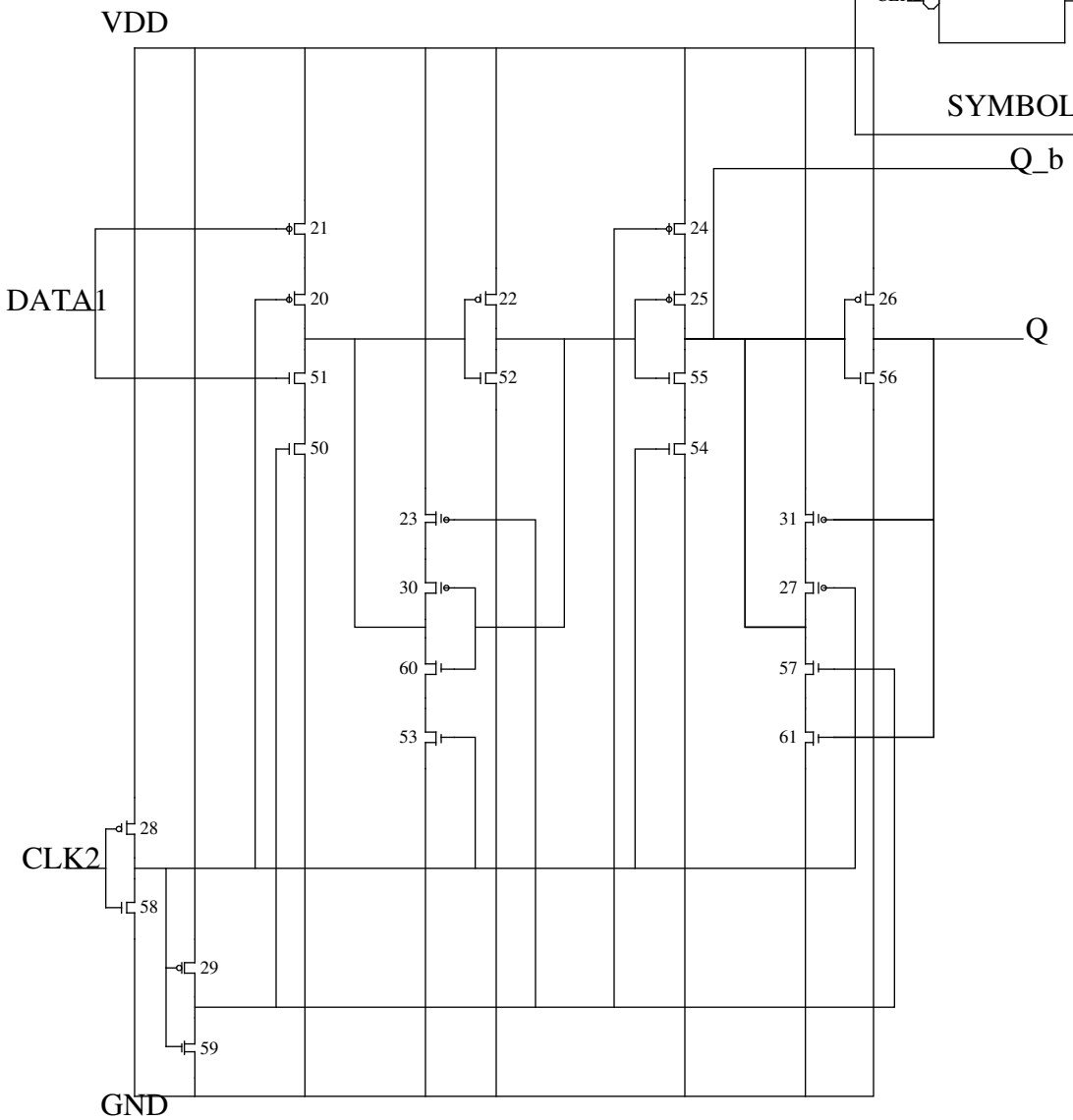
SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**dfnf311** D_FF_W/Q_&_Q'	DATE: Mar 11,1989 VERSION: dlmV2.0



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	FeedThru	----	----
2	CLK2	34	1
3	FeedThru	----	----
4	FeedThru	----	----
5	FeedThru	----	----
6	DATA1	38	0
7	FeedThru	----	----
8	Blocked		----
9	FeedThru	----	----
10	FeedThru	----	----
11	FeedThru	----	----
12	FeedThru	----	----
13	Q_b	20	0
14	Q	51	0
15	FeedThru	----	----

LOGIC EQUATIONS: Q = (Qn-1 * C) + (Dn-1 * C)'
Q=(.NOT.Q)'

Truth Table

C	D	Q	Q'
h	-	D	D'
l	-	Qn-1	Qn-1'