********** FLIP-FLOP TIMING INFO **********

2u SPECIAL FLIP FLOP TIMING

Data Setup time = 6.50 ns.

Data Hold time = 5.50 ns.

Maximum clock rise time

Clock pulse width = 3.50 ns.

Reset pulse width = 1.50 ns.

3u SPECIAL FLIP FLOP TIMING

Data Setup time = 13.50 ns.

Data Hold time = 9.50 ns.

Maximum clock rise time

Clock pulse width = 10.00 ns.

Reset pulse width = 7.00 ns.

********** SPICE DECK CONTINUED **********

```
M107x8 154 57 58 gnd NMOS W=12.0U L=2.0U
M115x8 58 27 155 gnd NMOS W=12.0U L=2.0U
M119x8 155 Q 156 gnd NMOS W=12.0U L=2.0U
M126x8 156 64 gnd gnd NMOS W=12.0U L=2.0U
M144x4 gnd 58 Q gnd NMOS W=18.0U L=2.0U
```

********** SPICE DECK **********

*** Generated from dfrf301.mag by magic's spice generator
*** technology: scmos
*** timestamp: 604100040
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M8x41 57 CLK2 vdd vdd PMOS W=29.0U L=2.0U
M16x41 vdd 57 27 vdd PMOS W=29.0U L=2.0U
M34x44 vdd DATA1 120 vdd PMOS W=26.0U L=2.0U
M38x44 120 57 52 vdd PMOS W=26.0U L=2.0U
M46x44 52 27 121 vdd PMOS W=22.0U L=2.0U
M54x44 121 24 vdd vdd PMOS W=22.0U L=2.0U
M62x44 vdd 64 121 vdd PMOS W=22.0U L=2.0U
M76x44 vdd 52 24 vdd PMOS W=22.0U L=2.0U
M96x45 vdd 24 123 vdd PMOS W=21.0U L=2.0U
M100x45 123 27 58 vdd PMOS W=21.0U L=2.0U
M114x45 vdd 57 124 vdd PMOS W=25.0U L=2.0U
M118x45 124 Q 58 vdd PMOS W=25.0U L=2.0U
M8x4 57 CLK2 gnd gnd NMOS W=24.0U L=2.0U
M16x4 gnd 57 27 gnd NMOS W=24.0U L=2.0U
M42x4 gnd DATA1 150 gnd NMOS W=19.0U L=2.0U
M46x4 150 27 52 gnd NMOS W=19.0U L=2.0U
M54x8 52 64 152 gnd NMOS W=15.0U L=2.0U
M58x8 152 24 151 gnd NMOS W=15.0U L=2.0U
M62x8 151 57 gnd gnd NMOS W=15.0U L=2.0U
M78x8 gnd 52 24 gnd NMOS W=15.0U L=2.0U
M126x39 58 64 vdd vdd PMOS W=31.0U L=2.0U
M144x39 vdd 58 Q vdd PMOS W=31.0U L=2.0U
M99x8 gnd 24 153 gnd NMOS W=12.0U L=2.0U
M103x8 153 64 154 gnd NMOS W=12.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
CLK2---Q	Pd 0--1	3.52	5.16	7.74	11.35
	Pd 1--0	3.48	5.28	7.66	11.62
	Tr 0--1	1.11	4.21	2.44	9.26
	Tf 1--0	1.05	2.94	2.31	6.47
RST3---Q	Pd 0--1	N/A	N/A	N/A	N/A
	Pd 1--0	1.25	2.63	2.75	5.79
	Tr 0--1	N/A	N/A	N/A	N/A
	Tf 1--0	1.16	2.90	2.55	6.38

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
CLK2---Q	Pd 0--1	11.21	13.91	18.06	21.54
	Pd 1--0	11.00	13.22	17.10	19.98
	Tr 0--1	4.37	8.62	5.87	11.67
	Tf 1--0	3.93	6.35	4.59	8.53
RST3---Q	Pd 0--1	N/A	N/A	N/A	N/A
	Pd 1--0	4.34	6.26	6.71	10.24
	Tr 0--1	N/A	N/A	N/A	N/A
	Tf 1--0	2.82	5.52	4.69	8.61

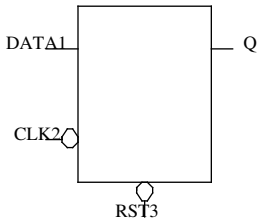
Cell Device Sizes

Transistor	Width (λ)	Length (λ)
62	24	2
63	24	2
51	19	2
50	19	2
55	15	2
54	15	2
53	15	2
52	15	2
56	12	2
61	12	2
59	12	2
60	12	2
58	18	2
57	12	2
64	12	2
33	29	2
32	29	2
20	26	2
21	26	2
25	22	2
23	22	2
22	22	2
27	21	2
26	21	2
31	25	2
29	25	2
30	31	2
28	31	2
24	22	2

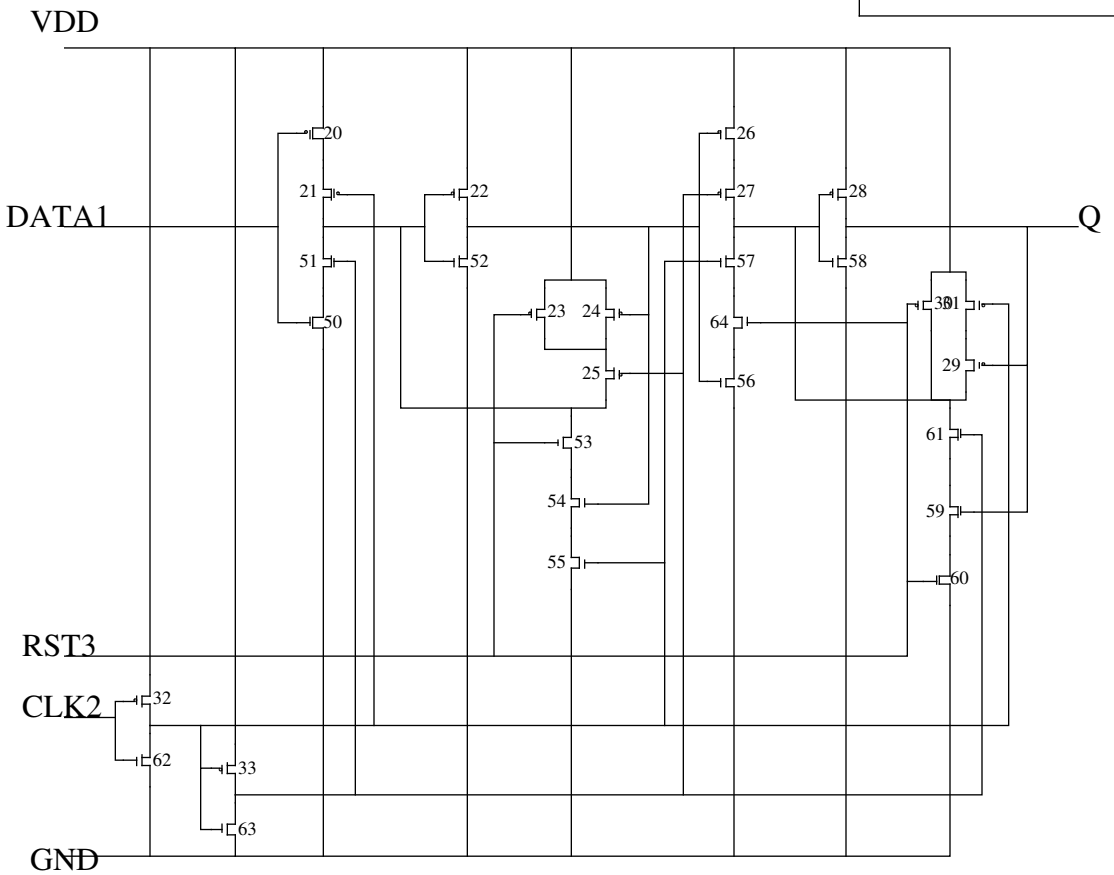
Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**dfrf301** D_FF_W/Q_&_ASY_RST	DATE: Mar 11,1989 VERSION: dlmV2.0



SYMBOL



LOGIC EQUATIONS: Q = [(Qn-1 * C) + (Dn-1 * C)]*R'

Truth Table

C	D	R	Q
l	-	1	Qn-1
h	-	1	D
-	-	0	0

Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**dfrf301** D_FF_W/Q_&_ASY_RST	DATE: Mar 11,1989 VERSION: dlmV2.0

TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	FeedThru	----	----
2	CLK2	24	1
3	FeedThru	----	----
4	DATA1	26	0
5	Blocked		----
6	Blocked		----
7	Blocked		----
8	FeedThru	----	----
9	FeedThru	----	----
10	Blocked		----
11	FeedThru	----	----
12	Blocked		----
13	Blocked		----
14	FeedThru	----	----
15	FeedThru	----	----
16	FeedThru	----	----
17	RST3	41	2
18	FeedThru	----	----
19	Q	31	0