********** SPICE DECK CONTINUED **********

```
M100x5 154 CIN2 55 gnd NMOS W=20.0U L=2.0U
M108x4 55 B1 152 gnd NMOS W=12.0U L=2.0U
M112x4 152 A1 gnd gnd NMOS W=12.0U L=2.0U
M120x1 gnd 55 CO gnd NMOS W=25.0U L=2.0U
```

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ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**faf001** FULL_ADDER	DATE: Dec 21,1988 VERSION: dlmV2.0

********** SPICE DECK **********

*** Generated from faf001.mag by magicsspicegenerator'
*** technology: scmos
*** timestamp: 598548127
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M12x38 SUM 63 vdd vdd PMOS W=29.0U L=2.0U
M20x38 vdd A1 120 vdd PMOS W=28.0U L=2.0U
M24x38 120 B1 121 vdd PMOS W=28.0U L=2.0U
M28x38 121 CIN2 63 vdd PMOS W=28.0U L=2.0U
M36x38 63 55 123 vdd PMOS W=25.0U L=2.0U
M44x38 123 CIN2 vdd vdd PMOS W=28.0U L=2.0U
M60x38 vdd B1 123 vdd PMOS W=29.0U L=2.0U
M68x39 123 A1 vdd vdd PMOS W=27.0U L=2.0U
M8x10 SUM 63 gnd gnd NMOS W=16.0U L=2.0U
M84x35 124 A1 vdd vdd PMOS W=31.0U L=2.0U
M92x35 vdd B1 124 vdd PMOS W=29.0U L=2.0U
M100x35 124 CIN2 55 vdd PMOS W=28.0U L=2.0U
M108x41 55 B1 122 vdd PMOS W=25.0U L=2.0U
M112x41 122 A1 vdd vdd PMOS W=25.0U L=2.0U
M120x41 vdd 55 CO vdd PMOS W=26.0U L=2.0U
M20x10 gnd A1 150 gnd NMOS W=10.0U L=2.0U
M24x10 150 B1 151 gnd NMOS W=10.0U L=2.0U
M28x10 151 CIN2 63 gnd NMOS W=10.0U L=2.0U
M36x9 63 55 153 gnd NMOS W=19.0U L=2.0U
M44x9 153 CIN2 gnd gnd NMOS W=19.0U L=2.0U
M60x1 gnd B1 153 gnd NMOS W=24.0U L=2.0U
M68x1 153 A1 gnd gnd NMOS W=16.0U L=2.0U
M84x1 154 A1 gnd gnd NMOS W=21.0U L=2.0U
M92x4 gnd B1 154 gnd NMOS W=21.0U L=2.0U

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1---SUM	Pd 0--1	12.45	14.62	19.95	23.13
	Pd 1--0	12.67	15.14	22.10	25.60
	Tr 0--1	4.74	9.60	5.78	12.56
	Tf 1--0	4.32	7.40	5.86	10.27
CIN2---SUM	Pd 0--1	11.22	13.54	18.51	22.91
	Pd 1--0	9.22	12.22	15.78	20.09
	Tr 0--1	4.78	9.29	7.34	11.88
	Tf 1--0	4.32	7.41	6.15	10.17
A1,B1---CO	Pd 0--1	8.79	11.88	16.80	20.70
	Pd 1--0	8.10	10.57	14.54	18.37
	Tr 0--1	4.07	9.21	7.36	12.37
	Tf 1--0	3.62	5.98	5.10	8.87
CIN2---CO	Pd 0--1	5.32	7.87	9.59	13.63
	Pd 1--0	6.68	8.84	12.13	15.61
	Tr 0--1	3.64	8.10	5.97	11.51
	Tf 1--0	3.48	5.08	5.96	7.69

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1---SUM	Pd 0--1	4.82	6.42	10.60	14.12
	Pd 1--0	4.88	6.53	10.74	14.37
	Tr 0--1	1.36	4.64	2.99	10.21
	Tf 1--0	1.85	3.72	4.07	8.18
CIN2---SUM	Pd 0--1	4.27	6.12	9.39	13.46
	Pd 1--0	3.55	5.45	7.81	11.99
	Tr 0--1	1.38	4.54	3.04	9.99
	Tf 1--0	1.26	3.84	2.77	8.45
A1,B1---CO	Pd 0--1	3.52	5.55	7.74	12.21
	Pd 1--0	3.41	4.96	7.50	10.91
	Tr 0--1	1.75	4.83	3.85	10.63
	Tf 1--0	1.26	2.99	2.77	6.58
CIN2---CO	Pd 0--1	1.99	3.93	4.38	8.65
	Pd 1--0	2.86	4.32	6.29	9.50
	Tr 0--1	1.11	4.82	2.44	10.60
	Tf 1--0	1.47	2.98	3.23	6.56

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
58	19	2
59	19	2
62	10	2
61	10	2
60	10	2
63	16	2
57	24	2
56	16	2
52	21	2
53	21	2
54	20	2
50	12	2
51	12	2
55	25	2
33	29	2
30	28	2
31	28	2
32	28	2
29	25	2
28	28	2
26	27	2
27	29	2
25	26	2
20	25	2
21	25	2
23	29	2
22	31	2
24	28	2

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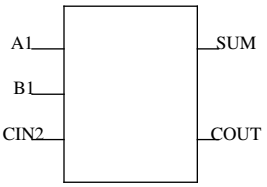
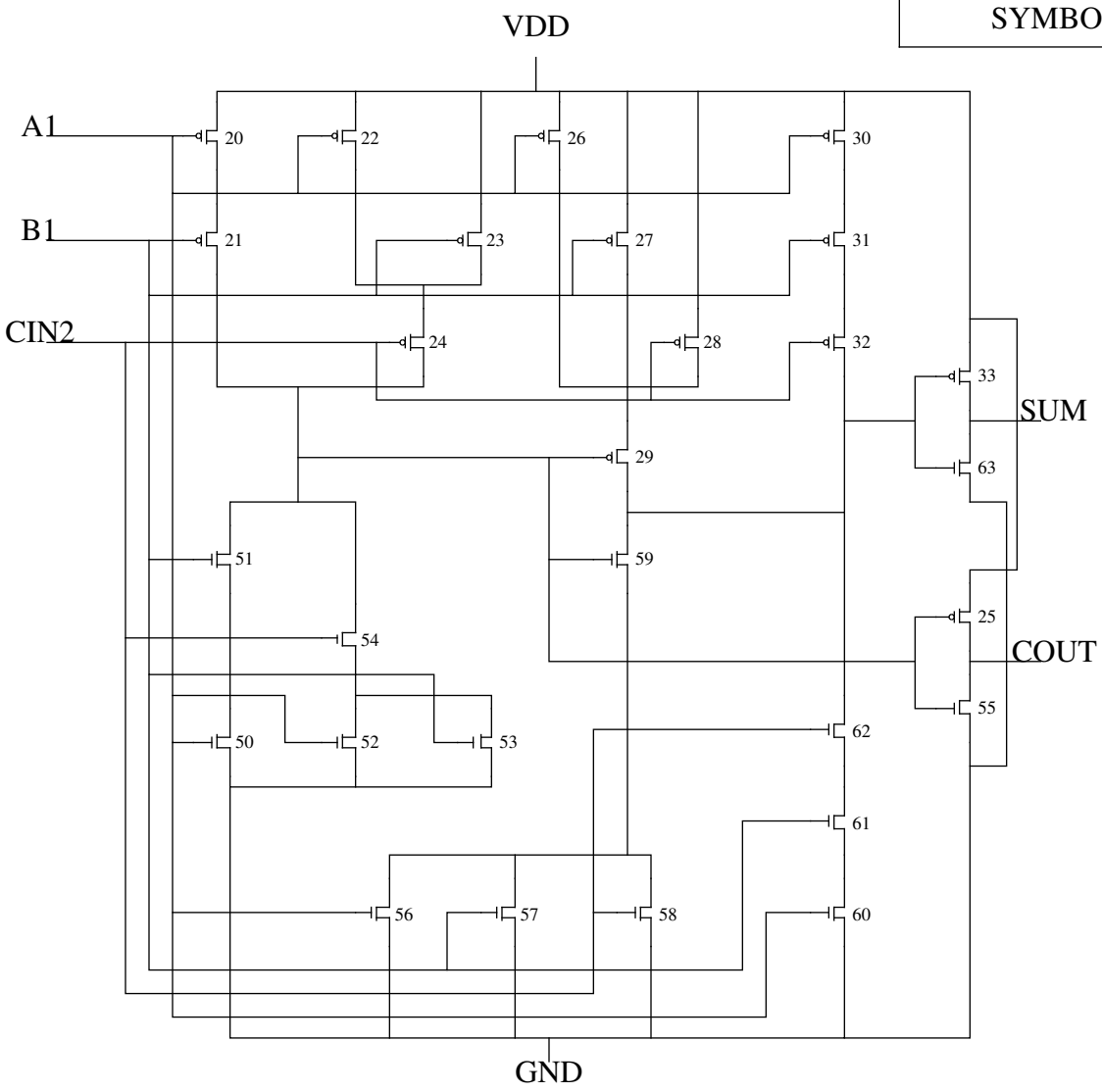


SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	SUM	41	0
2	FeedThru	----	----
3	FeedThru	----	----
4	FeedThru	----	----
5	FeedThru	----	----
6	FeedThru	----	----
7	FeedThru	----	----
8	FeedThru	----	----
9	CIN2	33	2
10	A1	20	1
11	B1	27	1
12	FeedThru	----	----
13	FeedThru	----	----
14	FeedThru	----	----
15	FeedThru	----	----
16	CO	35	0

LOGIC EQUATIONS: S = A xor B xor C
CO = AB xor AC xor BC

Truth Table

A	B	C	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1