********** SPICE DECK **********

*** Generated from invf100.mag by magicsspicegenerator'
*** technology: scmos
*** timestamp: 598319104
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M4x43 vdd 20 O vdd PMOS W=4.0U L=2.0U
M5x17 O 20 gnd gnd NMOS W=3.0U L=4.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	0.88	11.57	1.94	25.45
	Pd 1--0	0.92	11.50	2.02	25.30
	Tr 0--1	2.40	26.85	5.28	59.07
	Tf 1--0	2.38	21.81	5.24	47.98

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	2.47	16.37	3.93	28.11
	Pd 1--0	2.81	18.15	7.10	34.38
	Tr 0--1	5.16	38.68	10.57	53.12
	Tf 1--0	5.09	34.32	10.48	51.28

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SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**invf100** HI_Z_INVERTER	DATE: Dec 21,1988 VERSION: dlmV2.0

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	3	4
20	4	2

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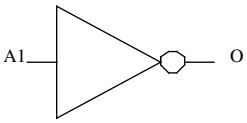
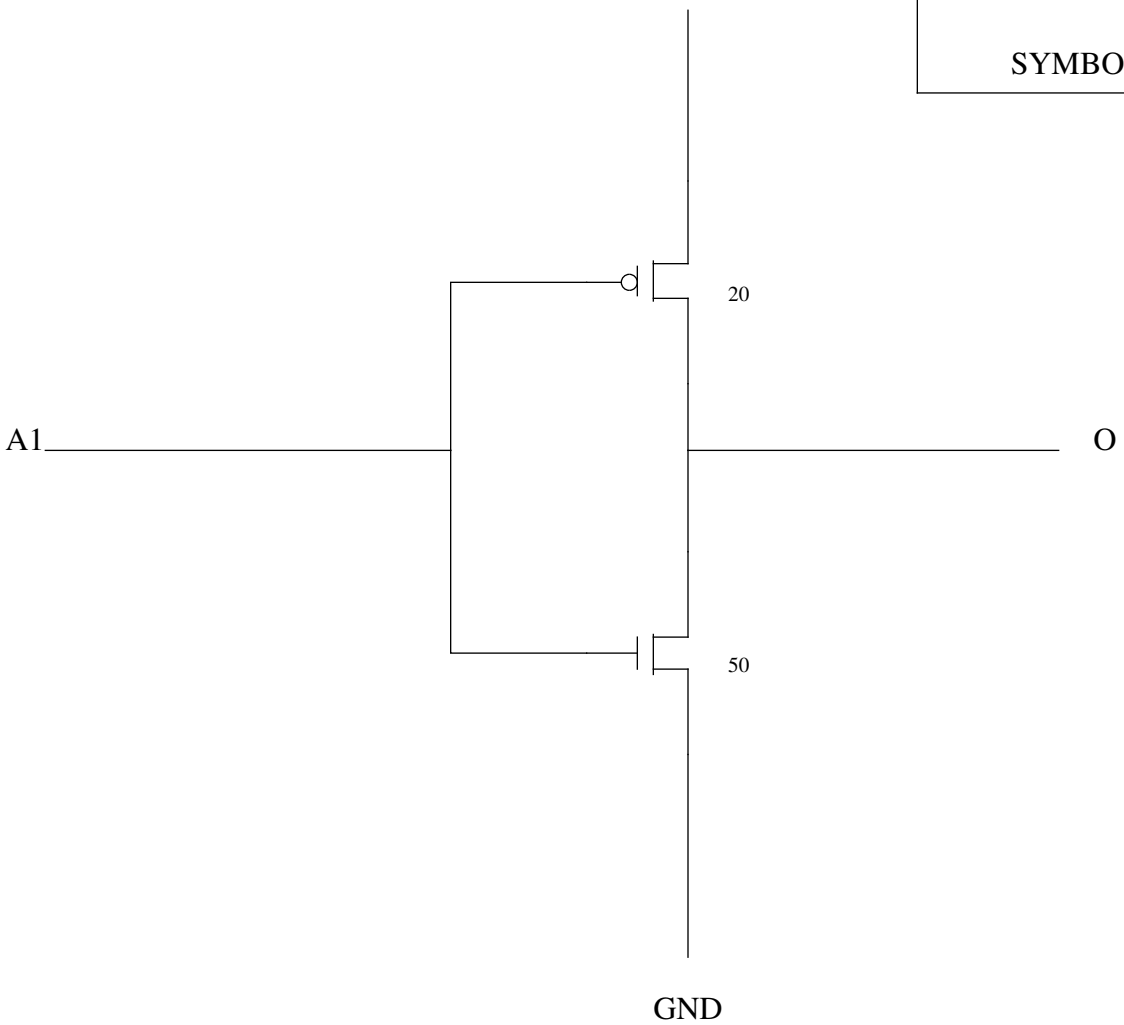


SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	O	30	0
2	A1	30	1

LOGIC EQUATIONS: O = A'

Truth Table

A	O
0	1