Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**invf101** INVERTER	DATE: Dec 21,1988 VERSION: dlmV2.0

********** SPICE DECK **********

*** Generated from invf101.mag by magic's spice generator
*** technology: scmos
*** timestamp: 598317966
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M8x41 vdd 50 O vdd PMOS W=26.0U L=2.0U
M8x8 gnd 50 O gnd NMOS W=12.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	0.58	3.23	1.28	7.11
	Pd 1--0	0.32	3.09	0.70	6.80
	Tr 0--1	1.96	5.66	4.31	12.45
	Tf 1--0	1.92	4.86	4.22	10.69

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	1.93	5.24	3.22	9.67
	Pd 1--0	1.08	4.58	3.17	9.91
	Tr 0--1	4.24	9.08	8.81	17.09
	Tf 1--0	3.90	7.45	8.83	14.69

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	12	2
20	26	2

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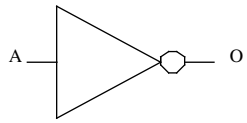
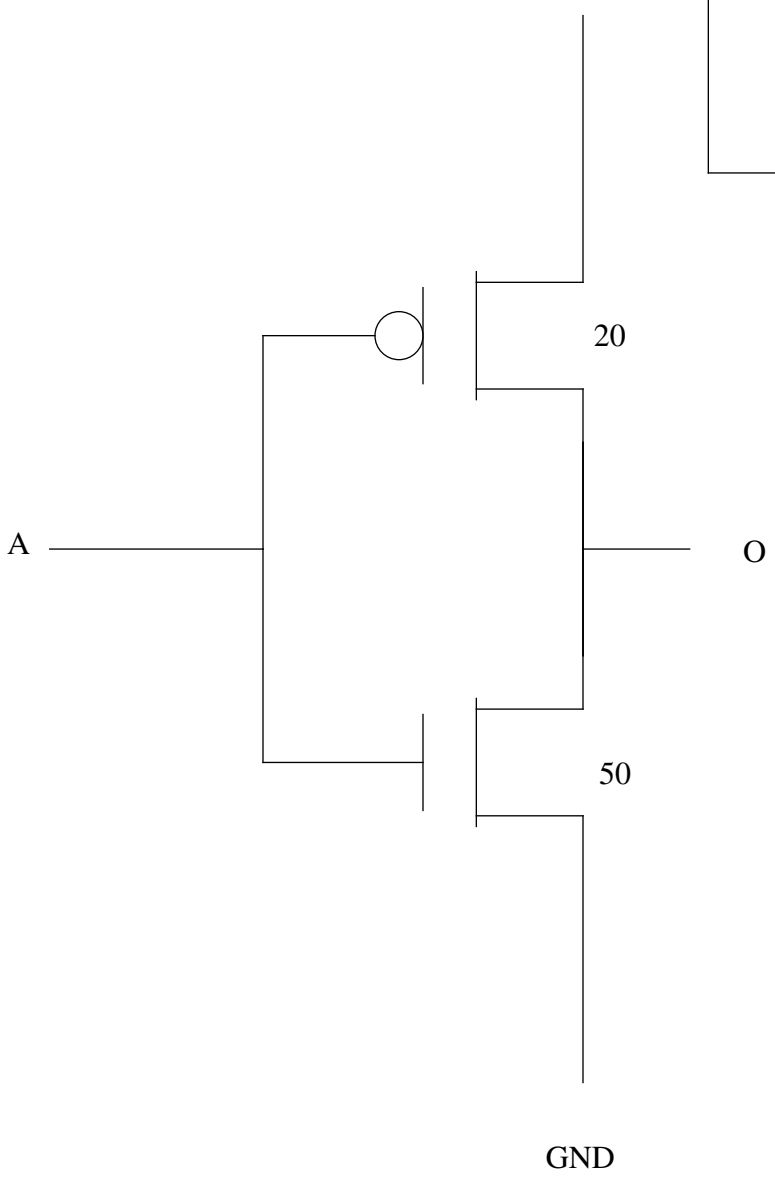


SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	A1	28	1
2	O	28	0

LOGIC EQUATIONS: O = A'

Truth Table

A	O
0	1