********** SPICE DECK **********

*** Generated from invf103.mag by magic's spice generator
*** technology: scmos
*** timestamp: 598556416
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M8x38 O 50 vdd vdd PMOS W=29.0U L=2.0U
M16x38 vdd 50 O vdd PMOS W=29.0U L=2.0U
M24x38 O 50 vdd vdd PMOS W=29.0U L=2.0U
M8x4 O 50 gnd gnd NMOS W=12.0U L=2.0U
M16x4 gnd 50 O gnd NMOS W=12.0U L=2.0U
M24x4 O 50 gnd gnd NMOS W=12.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	0.38	1.54	0.84	3.39
	Pd 1--0	0.35	1.55	0.77	3.41
	Tr 0--1	1.81	3.28	3.98	7.22
	Tf 1--0	1.78	3.09	3.92	6.80

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	1.50	2.94	2.20	5.08
	Pd 1--0	0.99	2.40	3.16	6.00
	Tr 0--1	4.11	5.80	8.63	11.21
	Tf 1--0	3.75	4.97	8.55	11.12

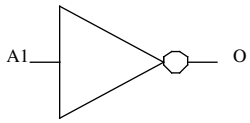
Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	36	2
20	87	2

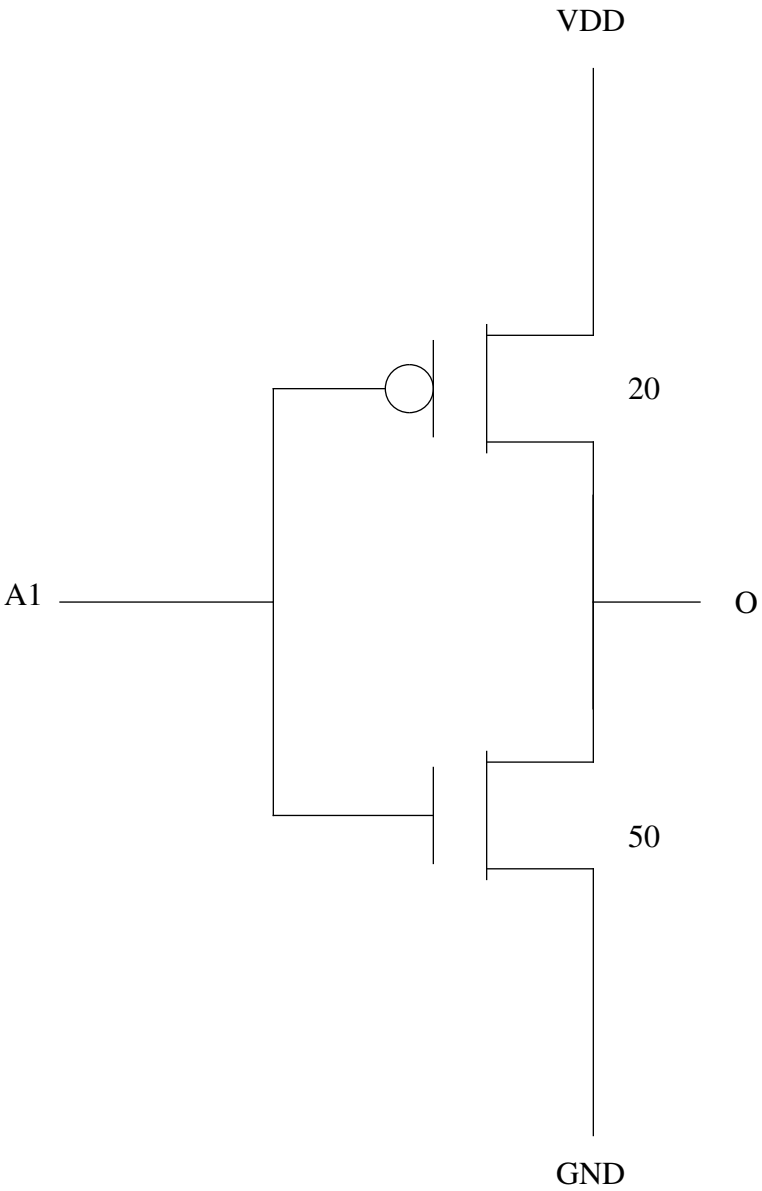
Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**invf103** 3X INVERTING BUFFER	DATE: Dec 21,1988 VERSION: dlmV2.0



SYMBOL



Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**invf103** 3X INVERTING BUFFER	DATE: Dec 21,1988 VERSION: dlmV2.0

TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	FeedThru	----	----
2	A1	22	1
3	O	32	0
4	FeedThru	----	----

LOGIC EQUATIONS: O= A'

Truth Table

A	O
0	1