Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**invf104** 4X_INVERTING_BUFFER	DATE: Dec 21,1988 VERSION: dlmV2.0

********** SPICE DECK **********

*** Generated from invf104.mag by magicsspicegenerator'
*** technology: scmos
*** timestamp: 598318851
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M8x38 vdd A1 O vdd PMOS W=29.0U L=2.0U
M16x38 O A1 vdd vdd PMOS W=29.0U L=2.0U
M24x38 vdd A1 O vdd PMOS W=29.0U L=2.0U
M32x38 O A1 vdd vdd PMOS W=29.0U L=2.0U
M8x1 gnd A1 O gnd NMOS W=12.0U L=2.0U
M16x1 O A1 gnd gnd NMOS W=12.0U L=2.0U
M24x1 gnd A1 O gnd NMOS W=12.0U L=2.0U
M32x1 O A1 gnd gnd NMOS W=12.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	0.36	1.31	0.79	2.88
	Pd 1--0	0.34	1.24	0.75	2.73
	Tr 0--1	1.80	2.99	3.96	6.58
	Tf 1--0	1.77	2.76	3.89	6.07

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	1.45	2.61	2.12	4.49
	Pd 1--0	0.96	2.12	3.12	5.51
	Tr 0--1	4.06	5.46	8.48	10.55
	Tf 1--0	3.73	4.52	8.52	10.61

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Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	48	2
20	116	2

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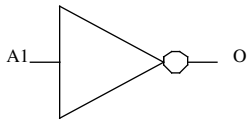
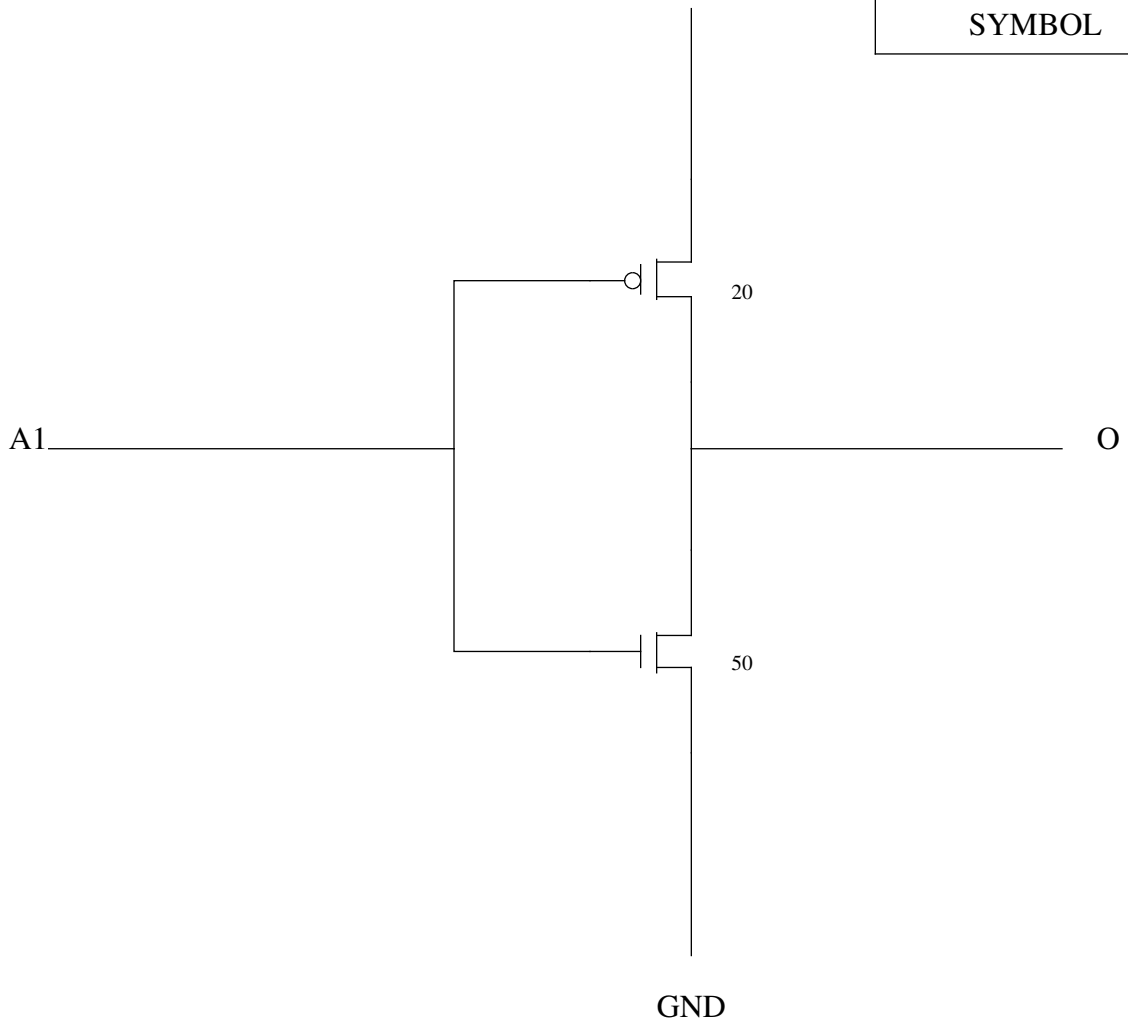


SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	FeedThru	----	----
2	O	30	0
3	FeedThru	----	----
4	A1	30	1
5	FeedThru	----	----

LOGIC EQUATIONS: O = A'

Truth Table

A	O
0	1