Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**invf201** DUAL_INVERTER	DATE: Dec 21,1988 VERSION: dlmV2.0

********** SPICE DECK **********

*** Generated from invf201.mag by magicsspicegenerator'
*** technology: scmos
*** timestamp: 598317966
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M8x38 O1 50 vdd vdd PMOS W=29.0U L=2.0U
M24x38 vdd 51 O2 vdd PMOS W=29.0U L=2.0U
M8x10 O1 50 gnd gnd NMOS W=13.0U L=2.0U
M24x10 gnd 51 O2 gnd NMOS W=13.0U L=2.0U

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O1	Pd 0--1	1.75	4.96	2.64	9.13
	Pd 1--0	1.18	4.19	3.50	9.51
	Tr 0--1	4.26	8.84	8.91	16.61
	Tf 1--0	3.94	7.14	8.84	14.44
B2---O1	Pd 0--1	N/A	N/A	N/A	N/A
	Pd 1--0	N/A	N/A	N/A	N/A
	Tr 0--1	N/A	N/A	N/A	N/A
	Tf 1--0	N/A	N/A	N/A	N/A
A1---O2	Pd 0--1	N/A	N/A	N/A	N/A
	Pd 1--0	N/A	N/A	N/A	N/A
	Tr 0--1	N/A	N/A	N/A	N/A
	Tf 1--0	N/A	N/A	N/A	N/A
B2---O2	Pd 0--1	1.75	4.96	2.64	9.13
	Pd 1--0	1.18	4.19	3.50	9.52
	Tr 0--1	4.26	8.85	8.91	16.62
	Tf 1--0	3.94	7.14	8.84	14.44

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O1	Pd 0--1	0.47	3.03	1.03	6.67
	Pd 1--0	0.44	2.82	0.97	6.20
	Tr 0--1	1.92	5.32	4.22	11.70
	Tf 1--0	1.84	4.70	4.05	10.34
B2---O1	Pd 0--1	N/A	N/A	N/A	N/A
	Pd 1--0	N/A	N/A	N/A	N/A
	Tr 0--1	N/A	N/A	N/A	N/A
	Tf 1--0	N/A	N/A	N/A	N/A
A1---O2	Pd 0--1	N/A	N/A	N/A	N/A
	Pd 1--0	N/A	N/A	N/A	N/A
	Tr 0--1	N/A	N/A	N/A	N/A
	Tf 1--0	N/A	N/A	N/A	N/A
B2---O2	Pd 0--1	0.47	3.03	1.03	6.67
	Pd 1--0	0.44	2.83	0.97	6.23
	Tr 0--1	1.92	5.32	4.22	11.70
	Tf 1--0	1.84	4.70	4.05	10.34

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	13	2
51	13	2
20	29	2
21	29	2

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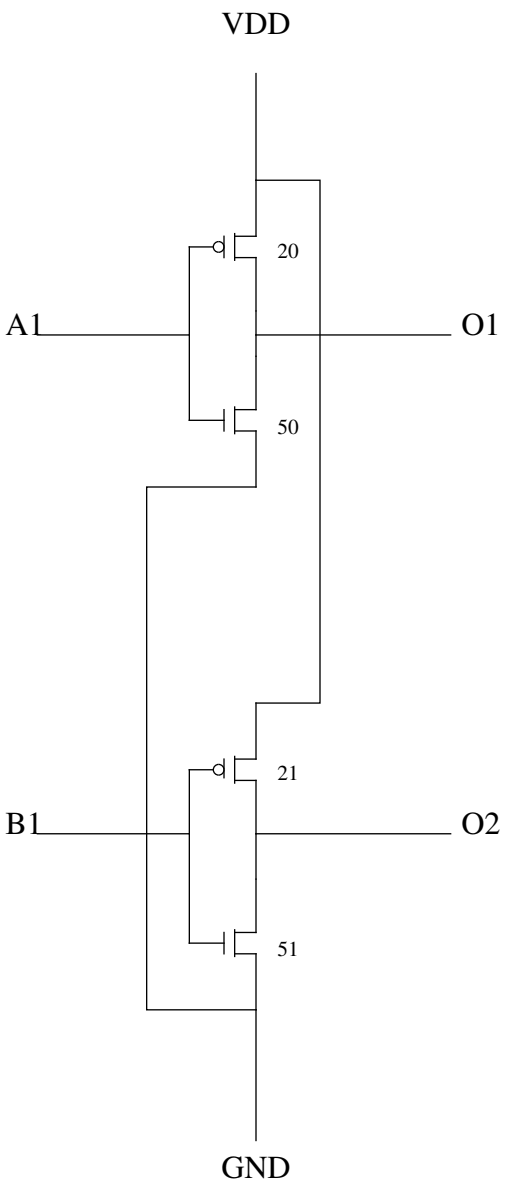

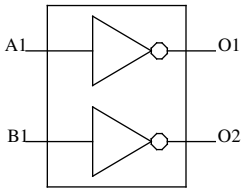

SYMBOL

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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	O1	28	0
2	A1	27	1
3	B2	27	2
4	O2	28	0

LOGIC EQUATIONS: O1 = A'
O2 = B'

Truth Table

A	B	O1	O2
0	-	1	0
-	0	0	1