Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**labf111** NAND_LATCH	DATE: Mar 11,1989 VERSION: dlmV2.0

********** SPICE DECK **********

*** Generated from labf111.mag by magic's spice generator
*** technology: scmos
*** timestamp: 604100040
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M12x41 vdd 23 21 vdd PMOS W=29.0U L=2.0U
M20x41 21 22 vdd vdd PMOS W=29.0U L=2.0U
M28x41 vdd 21 22 vdd PMOS W=29.0U L=2.0U
M36x41 22 20 vdd vdd PMOS W=29.0U L=2.0U
M16x4 21 23 150 gnd NMOS W=20.0U L=2.0U
M20x4 150 22 gnd gnd NMOS W=20.0U L=2.0U
M28x4 gnd 21 151 gnd NMOS W=20.0U L=2.0U
M32x4 151 20 22 gnd NMOS W=20.0U L=2.0U

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
SET2---Q	Pd 0--1	3.13	5.68	5.33	10.51
	Pd 1--0	2.18	5.17	5.28	10.56
	Tr 0--1	5.71	9.62	10.78	17.32
	Tf 1--0	5.29	9.13	11.47	16.95
RST1---Q	Pd 0--1	3.13	5.43	5.33	10.51
	Pd 1--0	4.67	9.52	6.90	17.21
	Tr 0--1	5.53	9.38	10.78	17.26
	Tf 1--0	3.78	7.57	4.39	11.60
SET2---Q_b	Pd 0--1	3.13	5.43	5.33	10.51
	Pd 1--0	4.67	9.52	6.90	17.21
	Tr 0--1	5.53	9.38	10.78	17.26
	Tf 1--0	3.78	7.57	4.39	11.60
RST1---Q_b	Pd 0--1	3.13	5.68	5.33	10.51
	Pd 1--0	2.18	5.17	5.28	10.56
	Tr 0--1	5.68	9.62	10.78	17.32
	Tf 1--0	5.29	9.13	11.47	16.95

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
SET2---Q	Pd 0--1	1.14	3.25	2.51	7.15
	Pd 1--0	0.58	2.86	1.28	6.29
	Tr 0--1	2.59	5.55	5.70	12.21
	Tf 1--0	2.45	5.34	5.39	11.75
RST1---Q	Pd 0--1	1.14	3.16	2.51	6.95
	Pd 1--0	1.44	5.54	3.17	12.19
	Tr 0--1	2.48	5.51	5.46	12.12
	Tf 1--0	1.23	4.53	2.71	9.97
SET2---Q_b	Pd 0--1	1.14	3.16	2.51	6.95
	Pd 1--0	1.44	5.54	3.17	12.19
	Tr 0--1	2.48	5.51	5.46	12.12
	Tf 1--0	1.23	4.53	2.71	9.97
RST1---Q_b	Pd 0--1	1.14	3.25	2.51	7.15
	Pd 1--0	0.58	2.86	1.28	6.29
	Tr 0--1	2.58	5.55	5.68	12.21
	Tf 1--0	2.44	5.34	5.37	11.75

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	20	2
51	20	2
52	20	2
53	20	2
22	29	2
21	29	2
20	29	2
23	29	2

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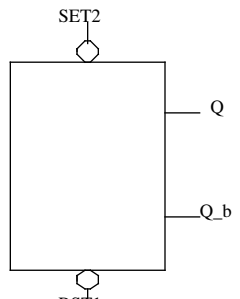
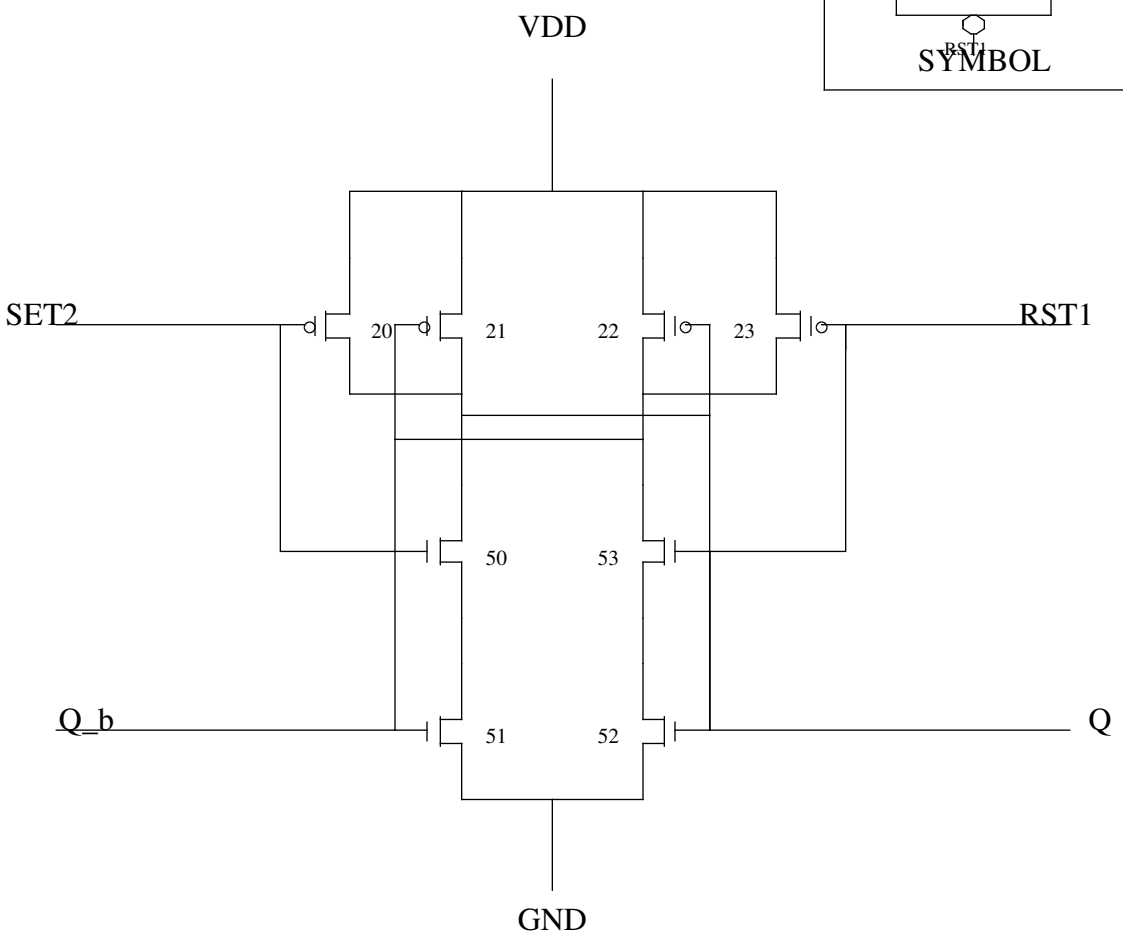


SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	RST1	33	2
2	Q_b	26	0
3	FeedThru	----	----
4	FeedThru	----	----
5	Q	26	0
6	SET2	33	1

LOGIC EQUATIONS: Q = (Qn-1 * S * R) + S'
Q=(Qn-1'*S*R)+R"

Truth Table

S	R	Q	Q'
0	0	1	1
0	1	1	0
1	0	0	1
1	1	Qn-1	Qn-1'
0	-	1	-
-	0	-	1