Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**labf211** NOR_LATCH	DATE: Dec 21,1988 VERSION: dlmV2.0

********** SPICE DECK **********

*** Generated from labf211.mag by magicsspicegenerator'
*** technology: scmos
*** timestamp: 598318477
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M12x30 23 SET2 120 vdd PMOS W=37.0U L=2.0U
M16x30 120 21 vdd vdd PMOS W=37.0U L=2.0U
M32x30 vdd 23 121 vdd PMOS W=37.0U L=2.0U
M36x30 121 RST1 21 vdd PMOS W=37.0U L=2.0U
M8x1 gnd SET2 23 gnd NMOS W=12.0U L=2.0U
M16x1 23 21 gnd gnd NMOS W=12.0U L=2.0U
M32x1 gnd 23 21 gnd NMOS W=12.0U L=2.0U
M40x1 21 RST1 gnd gnd NMOS W=12.0U L=2.0U

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
SET2---Q	Pd 0--1	5.12	11.01	9.34	19.09
	Pd 1--0	2.38	5.09	5.50	11.10
	Tr 0--1	5.31	11.68	7.14	16.94
	Tf 1--0	4.87	7.97	10.87	15.71
RST1---Q	Pd 0--1	3.77	7.15	5.78	12.00
	Pd 1--0	2.42	5.09	5.70	11.25
	Tr 0--1	7.20	12.58	12.88	22.38
	Tf 1--0	4.96	8.33	11.17	15.78
SET2---Q_b	Pd 0--1	3.77	7.14	5.78	12.00
	Pd 1--0	2.43	5.09	5.69	11.09
	Tr 0--1	7.21	12.57	12.88	22.37
	Tf 1--0	4.87	7.97	10.87	15.71
RST1---Q_b	Pd 0--1	5.11	11.01	9.34	19.09
	Pd 1--0	2.37	5.09	5.50	11.09
	Tr 0--1	5.27	11.68	7.14	16.94
	Tf 1--0	4.87	7.97	10.87	15.71

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
SET2---Q	Pd 0--1	1.67	6.48	3.67	14.26
	Pd 1--0	0.84	3.08	1.85	6.78
	Tr 0--1	2.03	6.76	4.47	14.87
	Tf 1--0	2.37	5.04	5.21	11.09
RST1---Q	Pd 0--1	1.32	4.06	2.90	8.93
	Pd 1--0	0.84	3.32	1.85	7.30
	Tr 0--1	3.01	7.12	6.62	15.66
	Tf 1--0	2.38	5.14	5.24	11.31
SET2---Q_b	Pd 0--1	1.32	4.06	2.90	8.93
	Pd 1--0	0.84	3.26	1.85	7.17
	Tr 0--1	3.04	7.12	6.69	15.66
	Tf 1--0	2.37	5.04	5.21	11.09
RST1---Q_b	Pd 0--1	1.67	6.48	3.67	14.26
	Pd 1--0	0.84	3.08	1.85	6.78
	Tr 0--1	2.03	6.76	4.47	14.87
	Tf 1--0	2.37	5.04	5.21	11.09

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	12	2
51	12	2
52	12	2
53	12	2
22	37	2
23	37	2
21	37	2
20	37	2

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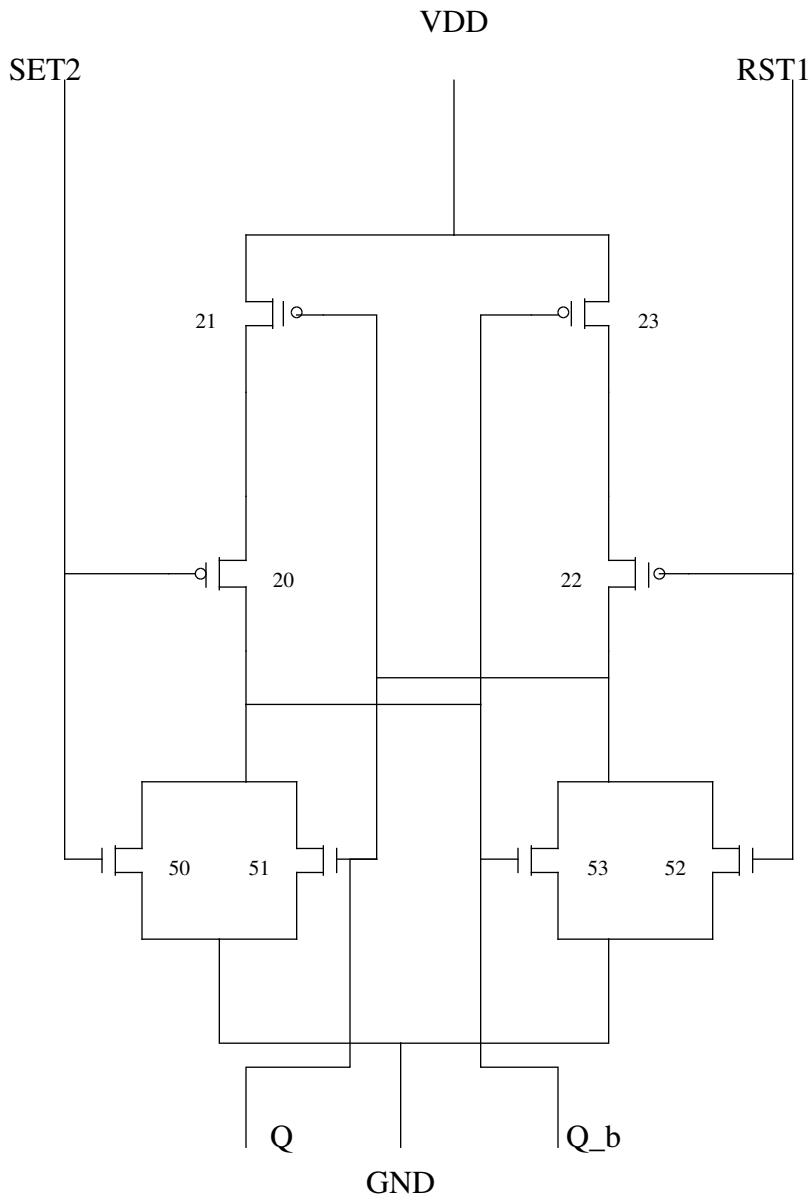

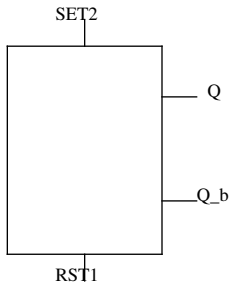

SYMBOL

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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	SET2	29	1
2	Q_b	22	0
3	FeedThru	----	----
4	FeedThru	----	----
5	Q	22	0
6	RST1	29	2

LOGIC EQUATIONS: Q = (S * R)+(Qn-1*S'*R')'
Q=(S'*R)+(Qn-1'*S'*R')'

Truth Table

S	R	Q	Q'
0	0	Qn-1	Qn-1'
0	1	0	1
1	0	1	0
1	1	0	0
1	-	-	0
-	1	0	-