********** SPICE DECK **********

*** Generated from larf310.mag by magic's spice generator
*** technology: scmos
*** timestamp: 604100040
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M8x45 51 50 vdd vdd PMOS W=16.0U L=2.0U
M16x45 vdd 51 53 vdd PMOS W=7.0U L=2.0U
M32x44 57 58 vdd vdd PMOS W=18.0U L=2.0U
M8x15 51 50 gnd gnd NMOS W=6.0U L=2.0U
M16x5 gnd 51 53 gnd NMOS W=16.0U L=2.0U
M48x44 vdd 57 120 vdd PMOS W=18.0U L=2.0U
M52x44 120 53 26 vdd PMOS W=18.0U L=2.0U
M60x43 26 51 Q vdd PMOS W=26.0U L=2.0U
M68x43 Q Q_b vdd vdd PMOS W=27.0U L=2.0U
M80x43 vdd 26 Q_b vdd PMOS W=27.0U L=2.0U
M88x49 Q_b 25 vdd vdd PMOS W=21.0U L=2.0U
M32x18 57 58 gnd gnd NMOS W=7.0U L=2.0U
M48x16 gnd 57 150 gnd NMOS W=9.0U L=2.0U
M52x16 150 51 26 gnd NMOS W=9.0U L=2.0U
M60x5 26 53 Q gnd NMOS W=24.0U L=2.0U
M68x4 Q Q_b gnd gnd NMOS W=25.0U L=2.0U
M84x4 gnd 26 151 gnd NMOS W=23.0U L=2.0U
M88x4 151 25 Q_b gnd NMOS W=23.0U L=2.0U

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
CLK2---Q	Pd 0--1	12.95	18.26	19.00	26.17
	Pd 1--0	11.63	15.69	18.33	24.12
	Tr 0--1	2.94	8.34	4.11	11.71
	Tf 1--0	2.77	5.40	3.35	7.38
DATA1---Q	Pd 0--1	11.23	16.68	17.91	25.21
	Pd 1--0	N/A	N/A	N/A	N/A
	Tr 0--1	3.16	8.35	4.04	11.34
	Tf 1--0	N/A	N/A	N/A	N/A
RST3---Q	Pd 0--1	N/A	N/A	N/A	N/A
	Pd 1--0	5.38	10.20	10.26	19.22
	Tr 0--1	N/A	N/A	N/A	N/A
	Tf 1--0	3.57	7.09	6.21	9.72
CLK2---Q_b	Pd 0--1	11.08	13.31	17.18	20.45
	Pd 1--0	10.99	13.08	16.55	19.80
	Tr 0--1	6.67	11.18	12.13	19.11
	Tf 1--0	4.86	8.11	5.88	11.07
DATA1---Q_b	Pd 0--1	N/A	N/A	N/A	N/A
	Pd 1--0	9.28	11.41	15.52	18.72
	Tr 0--1	N/A	N/A	N/A	N/A
	Tf 1--0	4.83	8.00	5.58	11.27
RST3---Q_b	Pd 0--1	4.43	7.13	8.33	13.69
	Pd 1--0	N/A	N/A	N/A	N/A
	Tr 0--1	6.67	11.18	12.13	19.11
	Tf 1--0	N/A	N/A	N/A	N/A

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
CLK2---Q	Pd 0--1	4.58	8.50	10.08	18.70
	Pd 1--0	4.42	7.62	9.72	16.76
	Tr 0--1	0.74	4.92	1.63	10.82
	Tf 1--0	0.65	3.17	1.43	6.97
DATA1---Q	Pd 0--1	4.14	8.07	9.11	17.75
	Pd 1--0	N/A	N/A	N/A	N/A
	Tr 0--1	0.75	4.92	1.65	10.82
	Tf 1--0	N/A	N/A	N/A	N/A
RST3---Q	Pd 0--1	N/A	N/A	N/A	N/A
	Pd 1--0	2.02	6.15	4.44	13.53
	Tr 0--1	N/A	N/A	N/A	N/A
	Tf 1--0	1.20	3.75	2.64	8.25
CLK2---Q_b	Pd 0--1	4.32	6.06	9.50	13.33
	Pd 1--0	4.13	5.57	9.09	12.25
	Tr 0--1	3.07	6.26	6.75	13.77
	Tf 1--0	1.70	4.04	3.74	8.89
DATA1---Q_b	Pd 0--1	N/A	N/A	N/A	N/A
	Pd 1--0	3.67	5.11	8.07	11.24
	Tr 0--1	N/A	N/A	N/A	N/A
	Tf 1--0	1.64	4.06	3.61	8.93
RST3---Q_b	Pd 0--1	1.86	4.26	4.09	9.37
	Pd 1--0	N/A	N/A	N/A	N/A
	Tr 0--1	3.07	6.26	6.75	13.77
	Tf 1--0	N/A	N/A	N/A	N/A

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
54	25	2
56	23	2
55	23	2
58	7	2
57	9	2
52	9	2
50	6	2
51	16	2
53	24	2
28	18	2
20	16	2
21	7	2
24	27	2
23	26	2
22	18	2
27	18	2
26	27	2
25	21	2

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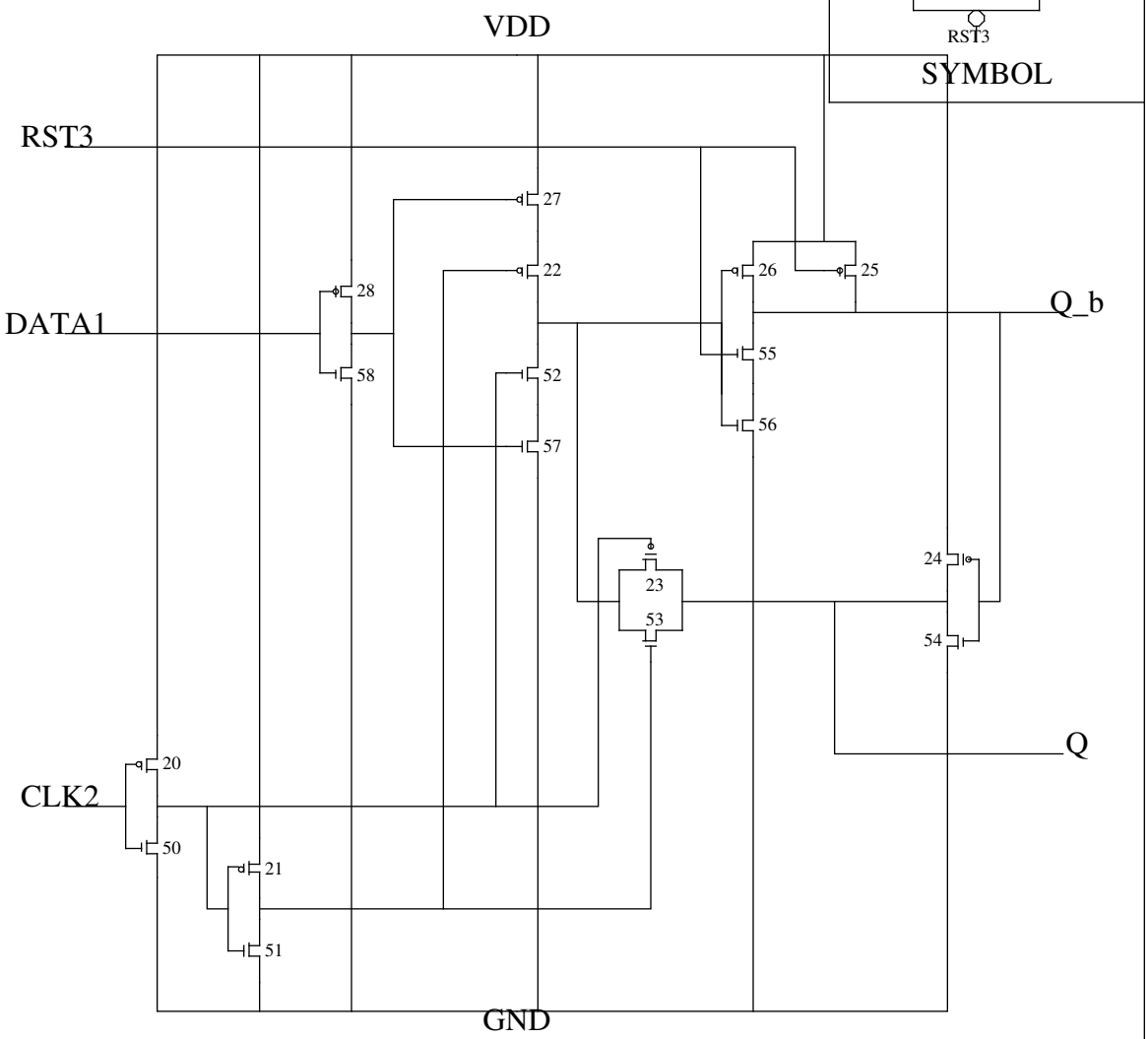
ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**larf310** CLOCKED_LATCH_W/RST	DATE: Mar 11,1989 VERSION: dlmV2.0



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	FeedThru	----	----
2	CLK2	25	1
3	FeedThru	----	----
4	FeedThru	----	----
5	DATA1	40	3
6	FeedThru	----	----
7	FeedThru	----	----
8	Q	33	0
9	FeedThru	----	----
10	FeedThru	----	----
11	Q_b	52	0
12	RST3	36	2

LOGIC EQUATIONS: Q = [(Qn-1 * C) + (D * C)]*R'
Q=(.NOT.Qn)'

Truth Table

C	D	R	Q	Q'
h2l	-	1	D	D'
l2h	-	1	Qn-1	Qn-1'
1	-	1	Qn-1	Qn-1'
0	0	1	0	1
0	1	1	1	0
-	-	0	0	1