********** SPICE DECK **********

*** Generated from nanf201.mag by magicsspicegenerator'
*** technology: scmos
*** timestamp: 598317966
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M12x36 vdd 50 O vdd PMOS W=31.0U L=2.0U
M20x36 O 51 vdd vdd PMOS W=31.0U L=2.0U
M12x3 gnd 50 150 gnd NMOS W=18.0U L=2.0U
M16x3 150 51 O gnd NMOS W=18.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1---O	Pd 0--1	0.74	3.02	1.63	6.64
	Pd 1--0	1.29	3.62	2.84	7.96
	Tr 0--1	2.39	5.64	5.26	12.41
	Tf 1--0	2.18	5.02	4.80	11.04

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1---O	Pd 0--1	2.60	5.17	4.55	9.66
	Pd 1--0	3.32	6.09	8.20	13.73
	Tr 0--1	5.32	9.12	10.59	16.78
	Tf 1--0	4.26	8.11	8.98	14.96

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	18	2
51	18	2
20	31	2
21	31	2

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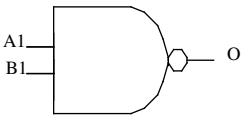
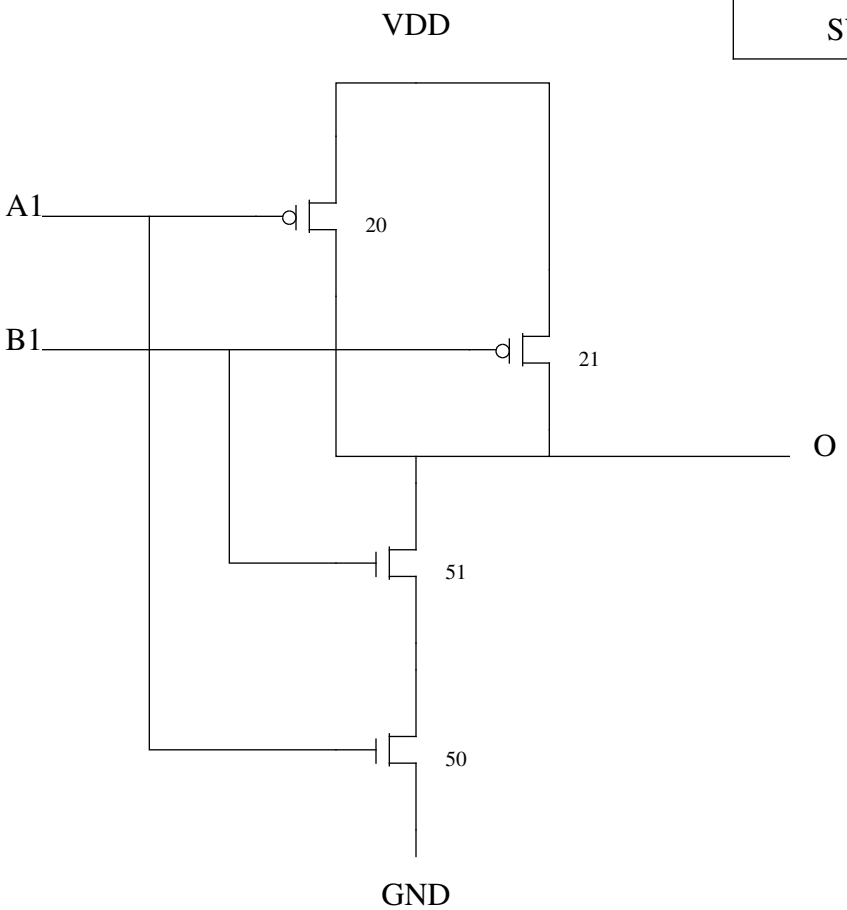
SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**nanf201** 2_INPUT_NAND	DATE: Dec 21,1988 VERSION: dlmV2.0



SYMBOL



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SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**nanf201** 2_INPUT_NAND	DATE: Dec 21,1988 VERSION: dlmV2.0

TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	A1	32	1
2	FeedThru	----	----
3	O	25	0
4	B1	32	1

LOGIC EQUATIONS: O = (A * B)'

Truth Table

A	B	O
0	-	1
-	0	1