********** SPICE DECK **********

*** Generated from nanf211.mag by magicsspicegenerator'
*** technology: scmos
*** timestamp: 598546947
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M8x43 vdd 51 52 vdd PMOS W=24.0U L=2.0U
M16x43 52 50 vdd vdd PMOS W=24.0U L=2.0U
M24x43 vdd 52 O2 vdd PMOS W=23.0U L=2.0U
M8x3 52 51 150 gnd NMOS W=16.0U L=2.0U
M12x3 150 50 gnd gnd NMOS W=16.0U L=2.0U
M24x10 gnd 52 O2 gnd NMOS W=9.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1---O1	Pd 0--1	1.22	3.63	2.68	7.99
	Pd 1--0	1.39	3.79	3.06	8.34
	Tr 0--1	2.67	6.27	5.87	13.79
	Tf 1--0	2.41	5.63	5.30	12.39
A1,B1---O2	Pd 0--1	1.65	6.96	3.63	15.31
	Pd 1--0	1.50	7.03	3.30	15.47
	Tr 0--1	0.86	5.73	1.89	12.61
	Tf 1--0	0.73	5.03	1.61	11.07

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1---O1	Pd 0--1	3.46	6.16	5.99	11.68
	Pd 1--0	3.49	6.52	8.51	14.39
	Tr 0--1	6.14	10.72	11.33	18.89
	Tf 1--0	5.17	9.34	10.22	16.53
A1,B1---O2	Pd 0--1	4.75	11.56	10.18	21.42
	Pd 1--0	4.62	11.12	8.13	19.94
	Tr 0--1	2.92	9.25	5.76	13.41
	Tf 1--0	2.70	7.00	3.36	10.46

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
52	9	2
51	16	2
50	16	2
21	24	2
20	24	2
22	23	2

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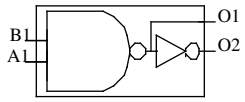
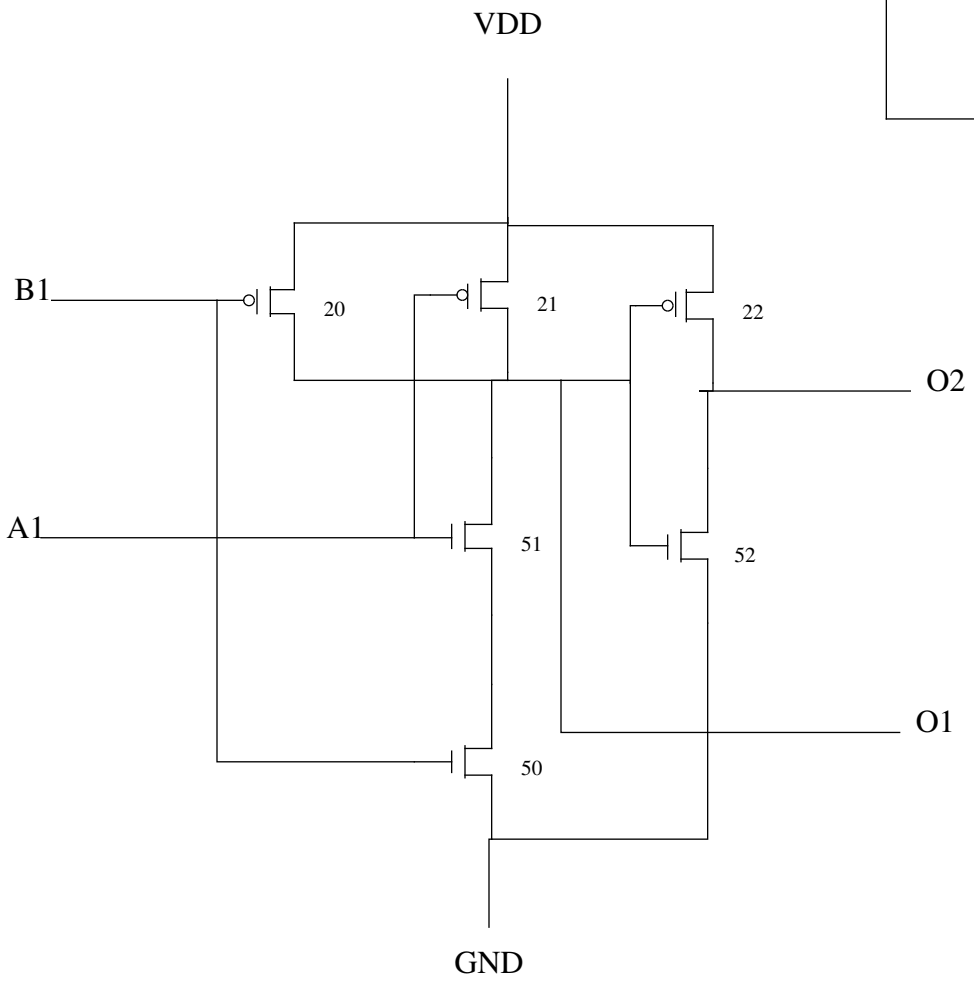
SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**nanf211** 2_INPUT_NAND/AND	DATE: Dec 21,1988 VERSION: dlmV2.0



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	A1	30	1
2	O1	37	0
3	B1	37	1
4	O2	37	0

LOGIC EQUATIONS: O1 = (A * B)'
O2 = A * B

Truth Table

A	B	O1	O2
0	-	1	0
-	0	1	0
1	1	0	1