Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**nanf251** A_OR_B'	DATE: Mar 11,1989 VERSION: dlmV2.0

********** SPICE DECK **********

*** Generated from nanf251.mag by magic's spice generator
*** technology: scmos
*** timestamp: 604100040
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M8x39 51 50 vdd vdd PMOS W=18.0U L=2.0U
M16x39 vdd 51 O vdd PMOS W=23.0U L=2.0U
M24x39 O 52 vdd vdd PMOS W=23.0U L=2.0U
M8x14 51 50 gnd gnd NMOS W=7.0U L=2.0U
M20x4 gnd 51 150 gnd NMOS W=17.0U L=2.0U
M24x4 150 52 O gnd NMOS W=17.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	1.94	4.18	4.27	9.20
	Pd 1--0	1.68	3.96	3.70	8.71
	Tr 0--1	1.83	5.06	4.03	11.13
	Tf 1--0	1.06	4.55	2.33	10.01
B2---O	Pd 0--1	0.75	3.55	1.65	7.81
	Pd 1--0	1.68	3.96	3.70	8.71
	Tr 0--1	2.12	6.09	4.66	13.40
	Tf 1--0	2.21	5.50	4.86	12.10

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	4.91	7.44	9.37	13.24
	Pd 1--0	4.53	7.29	8.66	13.90
	Tr 0--1	4.00	8.95	8.83	12.77
	Tf 1--0	3.41	7.32	5.38	12.46
B2---O	Pd 0--1	2.51	5.86	4.46	11.06
	Pd 1--0	4.53	7.29	8.66	13.90
	Tr 0--1	4.83	9.66	9.31	17.67
	Tf 1--0	4.60	9.11	9.81	17.22

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	7	2
52	17	2
51	17	2
20	18	2
21	23	2
22	23	2

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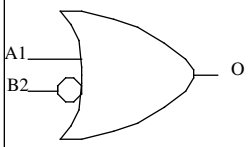
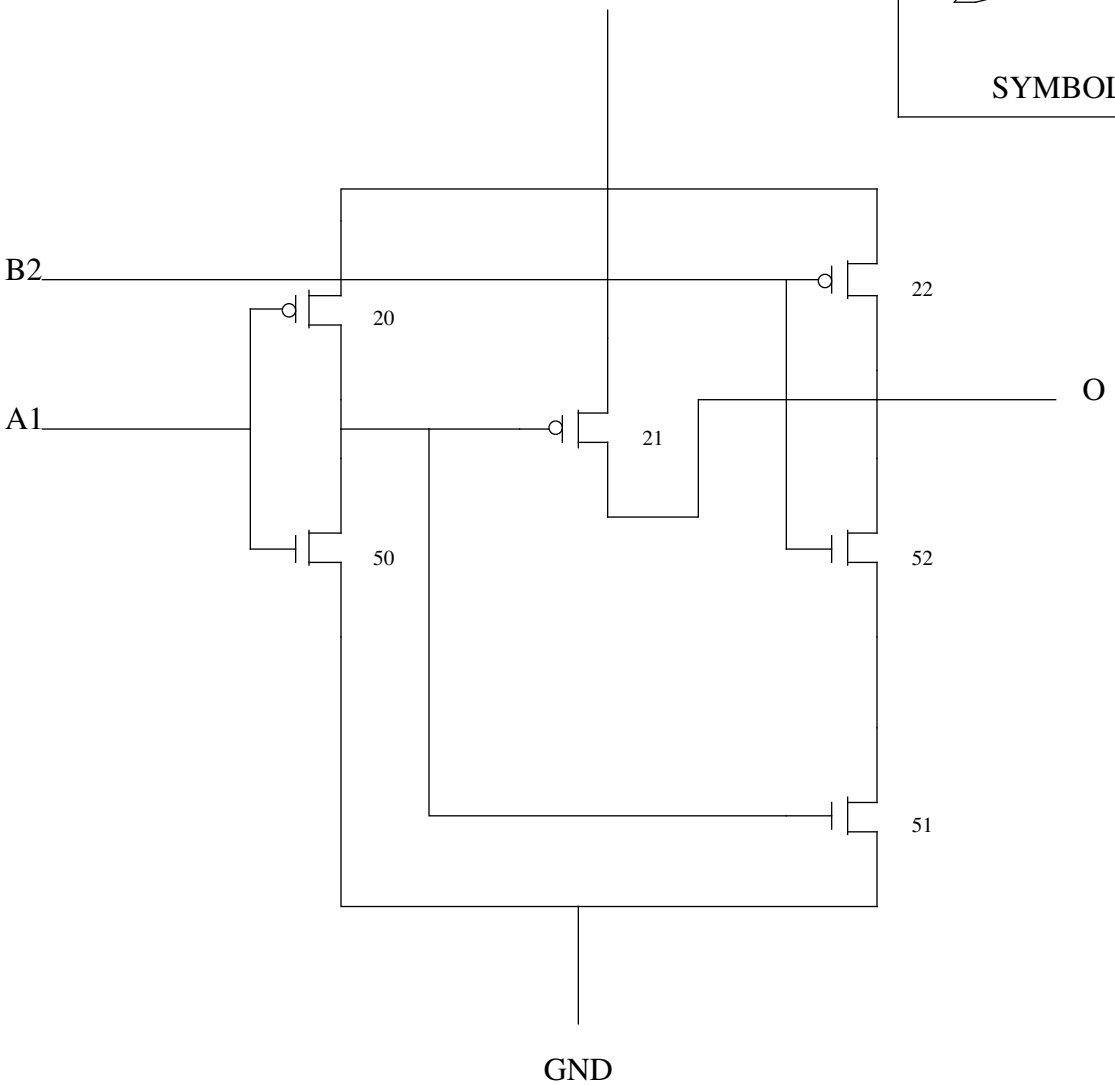


SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	FeedThru	----	----
2	A1	35	1
3	B2	33	2
4	O	35	0

LOGIC EQUATIONS: O = A + B'

Truth Table

A	B	O
-	0	1
1	-	1