Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**nanf301** 3_INPUT_NAND	DATE: Mar 11,1989 VERSION: dlmV2.0

********** SPICE DECK **********

*** Generated from nanf301.mag by magic's spice generator
*** technology: scmos
*** timestamp: 604100040
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M8x40 O A1 vdd vdd PMOS W=30.0U L=2.0U
M24x40 vdd 21 O vdd PMOS W=30.0U L=2.0U
M32x40 O C1 vdd vdd PMOS W=30.0U L=2.0U
M12x4 gnd A1 150 gnd NMOS W=25.0U L=2.0U
M16x4 150 21 151 gnd NMOS W=25.0U L=2.0U
M20x4 151 C1 O gnd NMOS W=25.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1,C1---O	Pd 0--1	1.51	3.35	3.32	7.37
	Pd 1--0	1.67	3.93	3.67	8.65
	Tr 0--1	3.11	5.74	6.84	12.63
	Tf 1--0	1.80	5.31	3.96	11.68

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1,C1---O	Pd 0--1	3.91	6.03	7.40	11.56
	Pd 1--0	4.58	7.31	11.06	15.89
	Tr 0--1	6.62	10.36	12.66	18.14
	Tf 1--0	5.31	9.38	9.49	16.45

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
51	25	2
52	25	2
50	25	2
22	30	2
20	30	2
21	30	2

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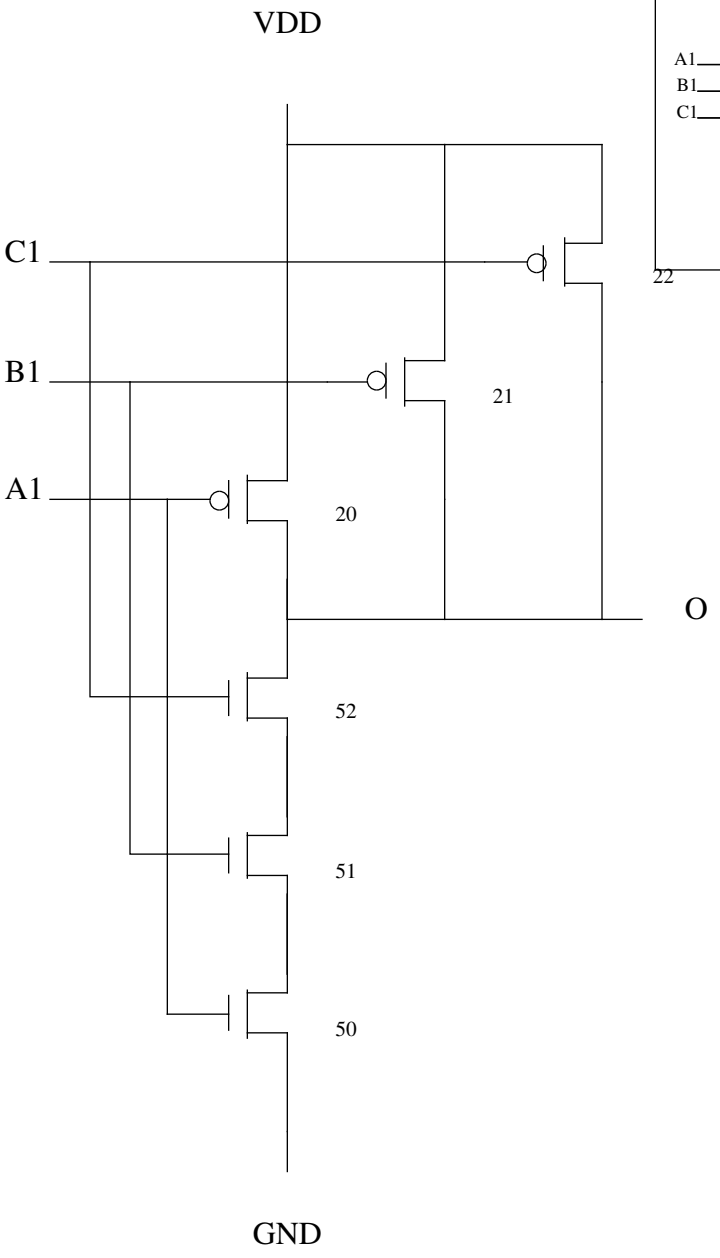

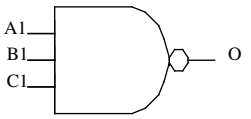

SYMBOL

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SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**nanf301** 3_INPUT_NAND	DATE: Mar 11,1989 VERSION: dlmV2.0

TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	A1	36	1
2	B1	36	1
3	FeedThru	----	----
4	O	47	0
5	C1	31	1

LOGIC EQUATIONS: O = (A * B * C)'

Truth Table

A	B	C	O
0	-	-	1
-	0	-	1
-	-	0	1