Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**nanf311** 3_INPUT_NAND/AND	DATE: Mar 11,1989 VERSION: dlmV2.0

********** SPICE DECK **********

*** Generated from nanf311.mag by magic's spice generator
*** technology: scmos
*** timestamp: 604100040
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M8x48 53 52 vdd vdd PMOS W=22.0U L=2.0U
M16x48 vdd 51 53 vdd PMOS W=22.0U L=2.0U
M24x48 53 A1 vdd vdd PMOS W=22.0U L=2.0U
M40x47 vdd 53 O2 vdd PMOS W=23.0U L=2.0U
M12x4 53 52 150 gnd NMOS W=23.0U L=2.0U
M16x4 150 51 151 gnd NMOS W=23.0U L=2.0U
M20x4 151 A1 gnd gnd NMOS W=23.0U L=2.0U
M36x13 gnd 53 O2 gnd NMOS W=14.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1,C1---O1	Pd 0--1	2.03	4.31	4.47	9.48
	Pd 1--0	1.89	4.22	4.16	9.28
	Tr 0--1	3.47	7.35	7.63	16.17
	Tf 1--0	2.45	6.06	5.39	13.33
A1,B1,C1---O2	Pd 0--1	2.31	7.63	5.08	16.79
	Pd 1--0	2.20	6.81	4.84	14.98
	Tr 0--1	1.54	5.92	3.39	13.02
	Tf 1--0	0.70	3.69	1.54	8.12

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1,C1---O1	Pd 0--1	4.88	7.50	9.34	14.30
	Pd 1--0	4.68	7.61	11.10	16.13
	Tr 0--1	7.91	13.34	14.09	21.90
	Tf 1--0	6.06	10.60	10.63	18.38
A1,B1,C1---O2	Pd 0--1	6.19	13.26	12.90	23.82
	Pd 1--0	5.39	11.28	10.61	20.56
	Tr 0--1	3.46	9.93	6.02	13.77
	Tf 1--0	1.80	5.28	2.95	8.62

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	23	2
51	23	2
52	23	2
53	14	2
20	22	2
23	23	2
22	22	2
21	22	2

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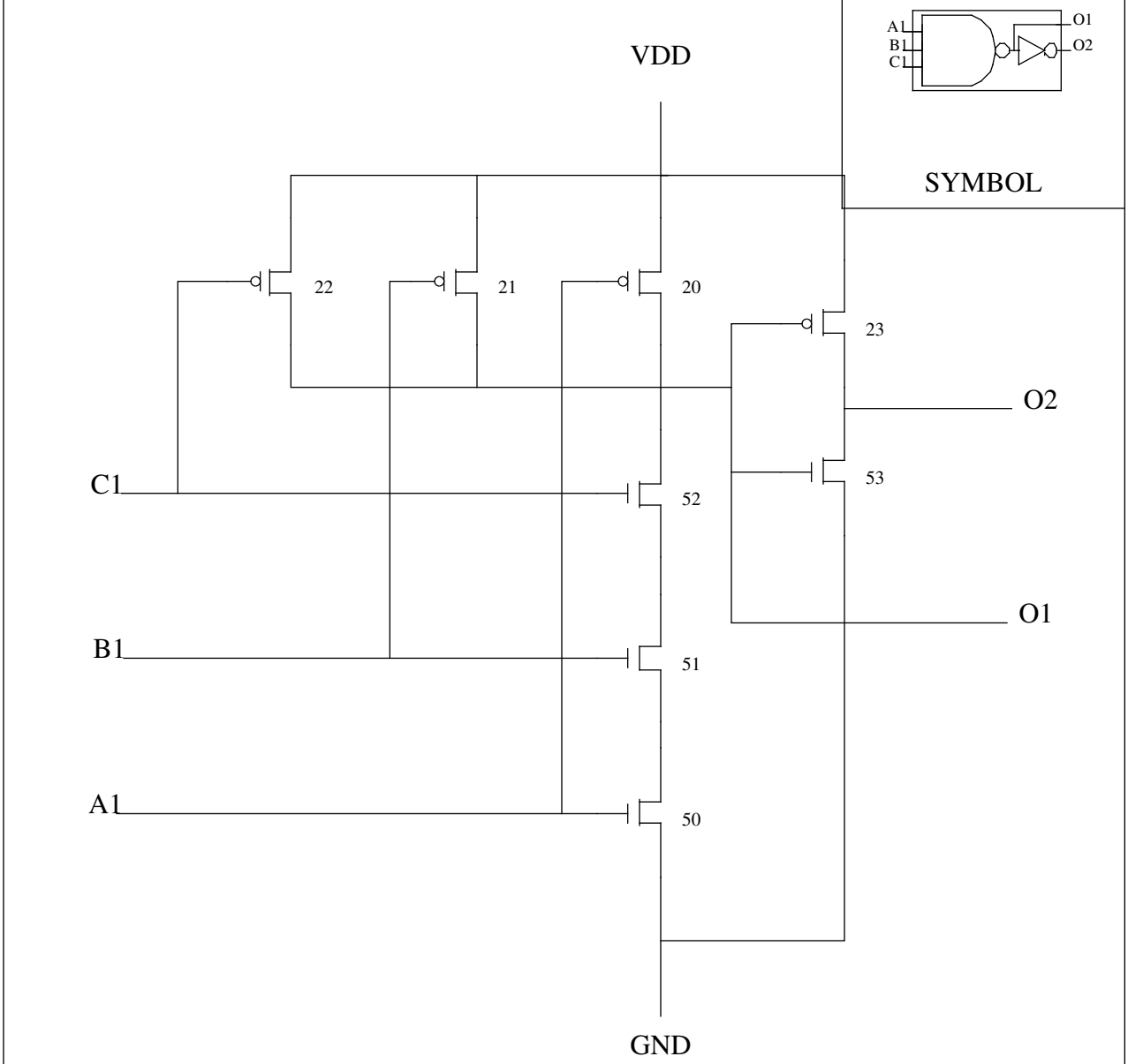

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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	FeedThru	----	----
2	C1	41	1
3	B1	41	1
4	A1	40	1
5	O1	34	0
6	O2	41	0

LOGIC EQUATIONS: O1 = (A * B * C)'
O2 = A * B * C

Truth Table

A	B	C	O1	O2
0	-	-	1	0
-	0	-	1	0
-	-	0	1	0
1	1	1	0	1