********** SPICE DECK **********

*** Generated from nanf401.mag by magic's spice generator
*** technology: scmos
*** timestamp: 604100040
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M8x48 vdd 53 O vdd PMOS W=22.0U L=2.0U
M16x48 O 52 vdd vdd PMOS W=22.0U L=2.0U
M24x48 vdd 51 O vdd PMOS W=22.0U L=2.0U
M32x48 O 50 vdd vdd PMOS W=22.0U L=2.0U
M16x4 O 53 150 gnd NMOS W=24.0U L=2.0U
M20x4 150 52 151 gnd NMOS W=24.0U L=2.0U
M24x4 151 51 152 gnd NMOS W=24.0U L=2.0U
M28x4 152 50 gnd gnd NMOS W=24.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1,C1,D1---O	Pd 0--1	1.89	4.12	4.16	9.06
	Pd 1--0	1.97	4.60	4.33	10.12
	Tr 0--1	3.46	7.01	7.61	15.42
	Tf 1--0	2.10	6.51	4.62	14.32

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1,C1,D1---O	Pd 0--1	4.70	7.40	9.03	14.07
	Pd 1--0	5.35	8.66	12.29	18.97
	Tr 0--1	8.10	12.83	14.16	21.88
	Tf 1--0	6.11	11.72	10.72	19.12

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
53	24	2
52	24	2
51	24	2
50	24	2
23	22	2
22	22	2
21	22	2
20	22	2

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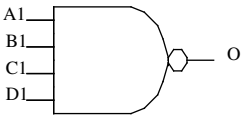
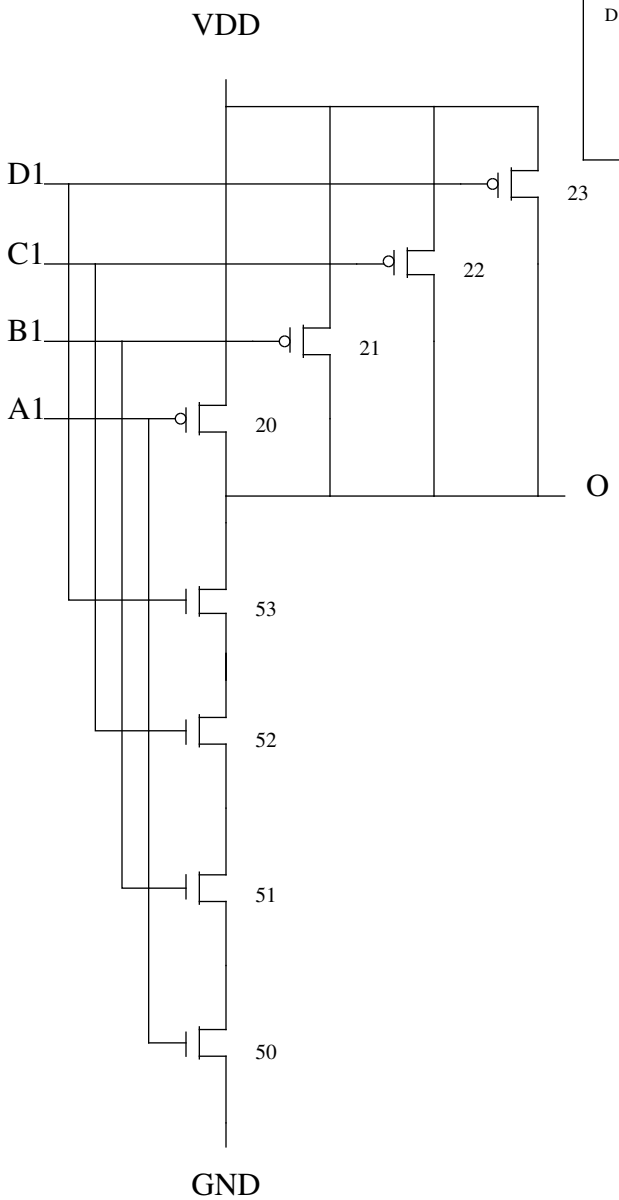
SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**nanf401** 4_INPUT_NAND	DATE: Mar 11,1989 VERSION: dlmV2.0



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	O	42	0
2	D1	42	1
3	C1	42	1
4	B1	42	1
5	A1	35	1

LOGIC EQUATIONS: O = (A * B * C * D)'

Truth Table

A	B	C	D	O
0	-	-	-	1
-	0	-	-	1
-	-	0	-	1
-	-	-	0	1