********** SPICE DECK **********

*** Generated from nanf411.mag by magicsspicegenerator'
*** technology: scmos
*** timestamp: 598549845
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M8x50 vdd D1 54 vdd PMOS W=17.0U L=2.0U
M16x50 54 C1 vdd vdd PMOS W=17.0U L=2.0U
M24x50 vdd B1 54 vdd PMOS W=17.0U L=2.0U
M32x50 54 A1 vdd vdd PMOS W=17.0U L=2.0U
M40x44 vdd 54 O2 vdd PMOS W=23.0U L=2.0U
M12x1 54 D1 150 gnd NMOS W=25.0U L=2.0U
M16x1 150 C1 151 gnd NMOS W=25.0U L=2.0U
M20x1 151 B1 152 gnd NMOS W=25.0U L=2.0U
M24x1 152 A1 gnd gnd NMOS W=25.0U L=2.0U
M40x1 gnd 54 O2 gnd NMOS W=17.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1,C1,D1---O1	Pd 0--1	2.57	5.10	5.65	11.22
	Pd 1--0	1.96	4.56	4.31	10.03
	Tr 0--1	3.87	8.98	8.51	19.76
	Tf 1--0	2.28	6.58	5.02	14.48
A1,B1,C1,D1---O2	Pd 0--1	2.38	8.20	5.24	18.04
	Pd 1--0	2.67	7.41	5.87	16.30
	Tr 0--1	1.90	6.30	4.18	13.86
	Tf 1--0	0.73	3.20	1.61	7.04

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1,C1,D1---O1	Pd 0--1	6.04	9.26	11.79	17.10
	Pd 1--0	5.31	8.45	12.15	18.61
	Tr 0--1	9.63	16.95	15.67	25.73
	Tf 1--0	6.67	12.17	11.93	20.10
A1,B1,C1,D1---O2	Pd 0--1	7.05	14.74	14.58	26.61
	Pd 1--0	6.61	12.68	12.59	22.81
	Tr 0--1	3.57	10.63	6.29	14.56
	Tf 1--0	1.84	4.84	3.03	8.07

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	25	2
51	25	2
52	25	2
53	25	2
54	17	2
23	17	2
22	17	2
21	17	2
20	17	2
24	23	2

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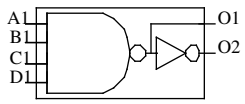
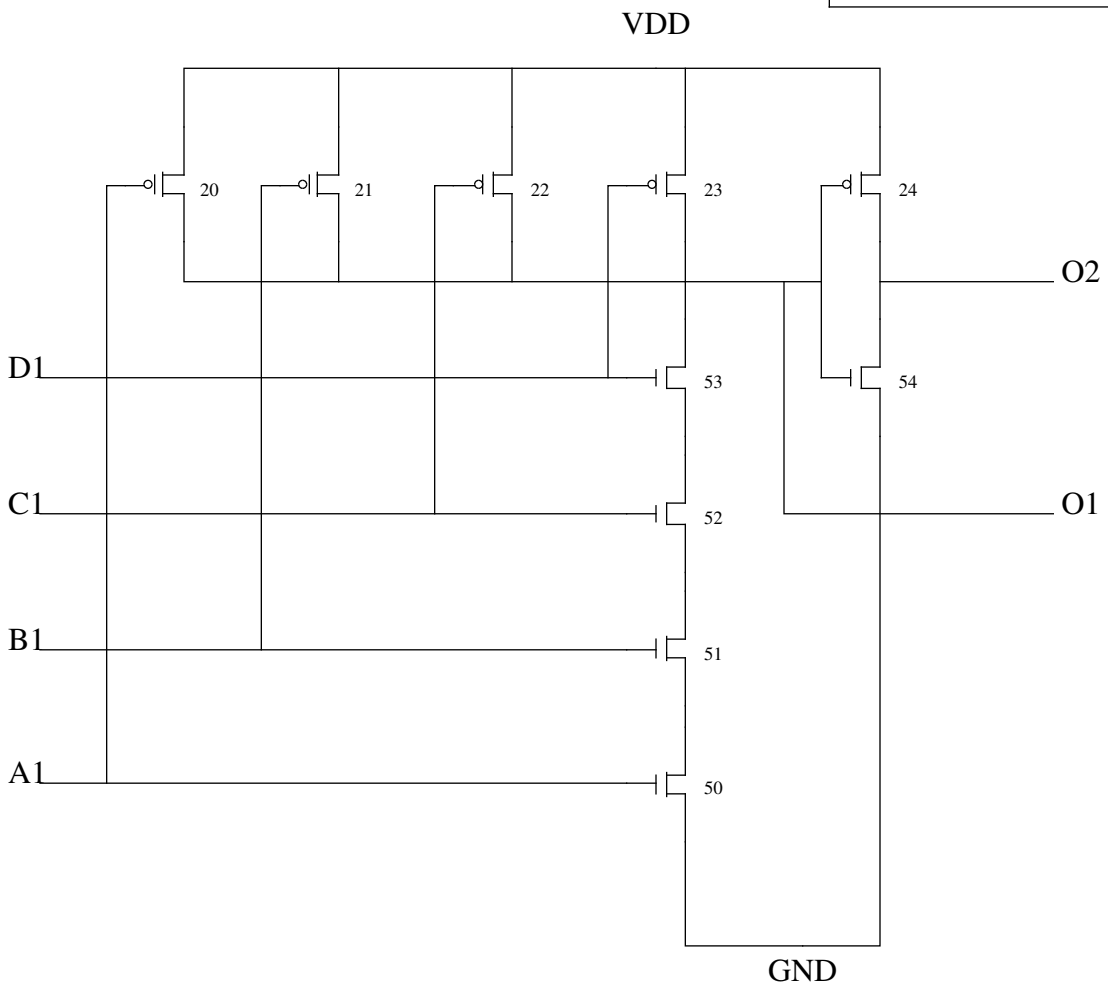
SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**nanf411** 4_INPUT_NAND/AND	DATE: Dec 21,1988 VERSION: dlmV2.0



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	D1	24	1
2	C1	39	1
3	O1	45	0
4	B1	39	1
5	A1	30	1
6	O2	31	0

LOGIC EQUATIONS: O1 = (A * B * C * D)'
O2 = A * B * C * D

Truth Table

A	B	C	D	O1	O2
0	-	-	-	1	0
-	0	-	-	1	0
-	-	0	-	1	0
-	-	-	0	1	0
1	1	1	1	0	1