********** SPICE DECK **********

*** Generated from oaif2201.mag by magicsspicegenerator'
*** technology: scmos
*** timestamp: 598548197
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M12x41 vdd 50 120 vdd PMOS W=26.0U L=2.0U
M16x41 120 51 O vdd PMOS W=26.0U L=2.0U
M24x41 O 52 121 vdd PMOS W=26.0U L=2.0U
M28x41 121 53 vdd vdd PMOS W=26.0U L=2.0U
M8x10 150 50 gnd gnd NMOS W=9.0U L=2.0U
M16x10 gnd 51 150 gnd NMOS W=9.0U L=2.0U
M24x5 150 52 O gnd NMOS W=14.0U L=2.0U
M32x5 O 53 150 gnd NMOS W=14.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1---O	Pd 0--1	1.74	5.22	3.83	11.48
	Pd 1--0	2.12	4.96	4.66	10.91
	Tr 0--1	3.93	10.18	8.65	22.40
	Tf 1--0	2.49	7.42	5.48	16.32
C2,D2---O	Pd 0--1	1.72	5.22	3.78	11.48
	Pd 1--0	2.12	4.96	4.66	10.91
	Tr 0--1	3.86	10.18	8.49	22.40
	Tf 1--0	2.49	7.42	5.48	16.32

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1---O	Pd 0--1	5.08	9.58	8.44	15.82
	Pd 1--0	5.17	8.53	11.94	18.52
	Tr 0--1	10.18	19.40	16.28	29.10
	Tf 1--0	6.06	12.60	11.96	20.42
C2,D2---O	Pd 0--1	4.96	9.56	7.60	15.64
	Pd 1--0	5.17	8.53	11.94	18.52
	Tr 0--1	10.18	19.39	15.81	29.10
	Tf 1--0	6.06	12.60	11.96	20.42

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
53	14	2
52	14	2
51	9	2
50	9	2
20	26	2
21	26	2
23	26	2
22	26	2

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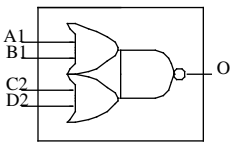
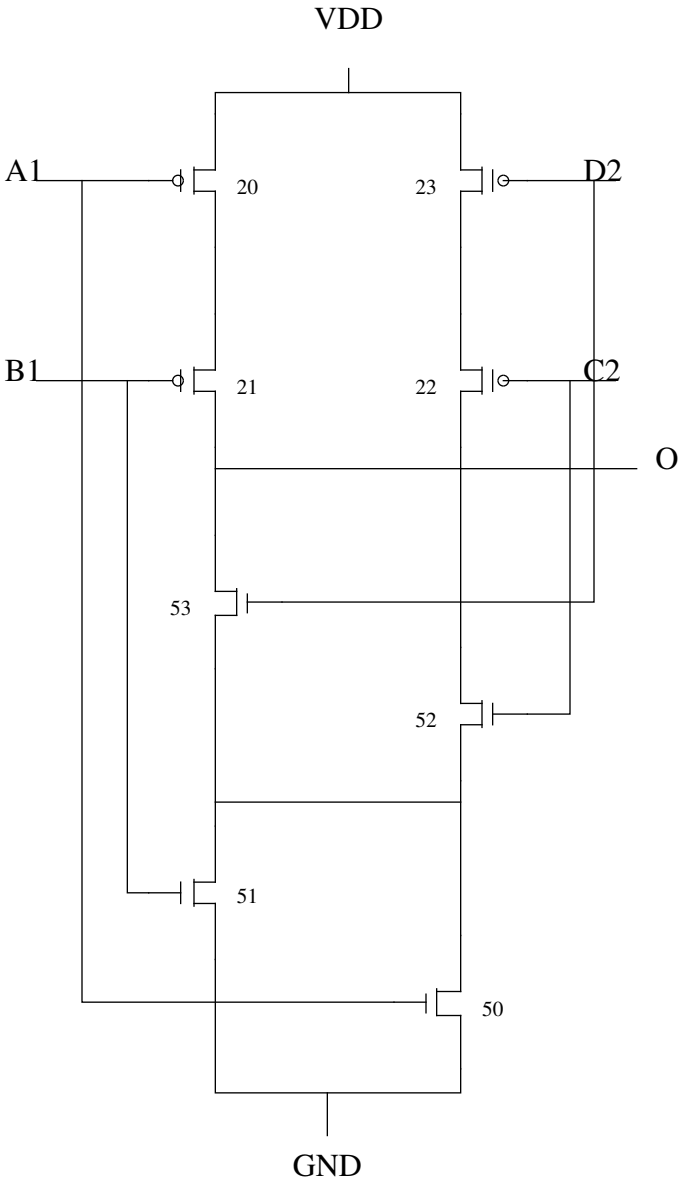
SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**oaif2201** 2/2_OR/NAND_MUX	DATE: Dec 21,1988 VERSION: dlmV2.0



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	A1	25	1
2	B1	27	1
3	C2	25	2
4	O	24	0
5	D2	29	2

LOGIC EQUATIONS: O = ((A+B) * (C+D))'

Truth Table

A	B	C	D	O
0	0	-	-	1
-	-	0	0	1