Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL FAMILY	**swcf020** TRANSMISSION_GATE	DATE: Dec 21,1988 VERSION: dlmV2.0

********** SPICE DECK **********

*** Generated from swcf020.mag by magicsspicegenerator'
*** technology: scmos
*** timestamp: 598318136
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M8x46 20 CTL2 vdd vdd PMOS W=21.0U L=2.0U
M24x36 O 20 DATA1 vdd PMOS W=31.0U L=2.0U
M32x36 DATA1 20 O vdd PMOS W=31.0U L=2.0U
M8x1 20 CTL2 gnd gnd NMOS W=18.0U L=2.0U
M24x1 O CTL2 DATA1 gnd NMOS W=24.0U L=2.0U
M32x1 DATA1 CTL2 O gnd NMOS W=24.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
DATA1---O	Pd 0--1	0.10	0.43	0.22	0.95
	Pd 1--0	0.10	0.50	0.22	1.10
	Tr 0--1	6.10	6.51	13.42	14.32
	Tf 1--0	5.93	5.80	13.05	12.76
CTL2---O	Pd 0--1	0.12	1.01	0.26	2.22
	Pd 1--0	0.00	0.26	0.00	0.57
	Tr 0--1	2.60	3.32	5.72	7.30
	Tf 1--0	1.40	2.93	3.08	6.45

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
DATA1---O	Pd 0--1	0.39	0.96	0.74	1.83
	Pd 1--0	0.42	1.13	0.78	2.06
	Tr 0--1	10.44	11.29	30.47	31.35
	Tf 1--0	9.76	9.54	29.58	28.89
CTL2---O	Pd 0--1	1.22	2.51	2.95	4.96
	Pd 1--0	0.00	0.56	0.00	0.46
	Tr 0--1	5.84	6.72	11.17	11.41
	Tf 1--0	3.68	4.78	8.11	10.69

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
51	18	2
50	48	2
20	62	2
21	21	2

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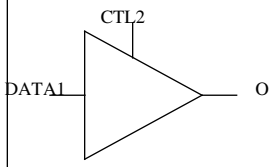
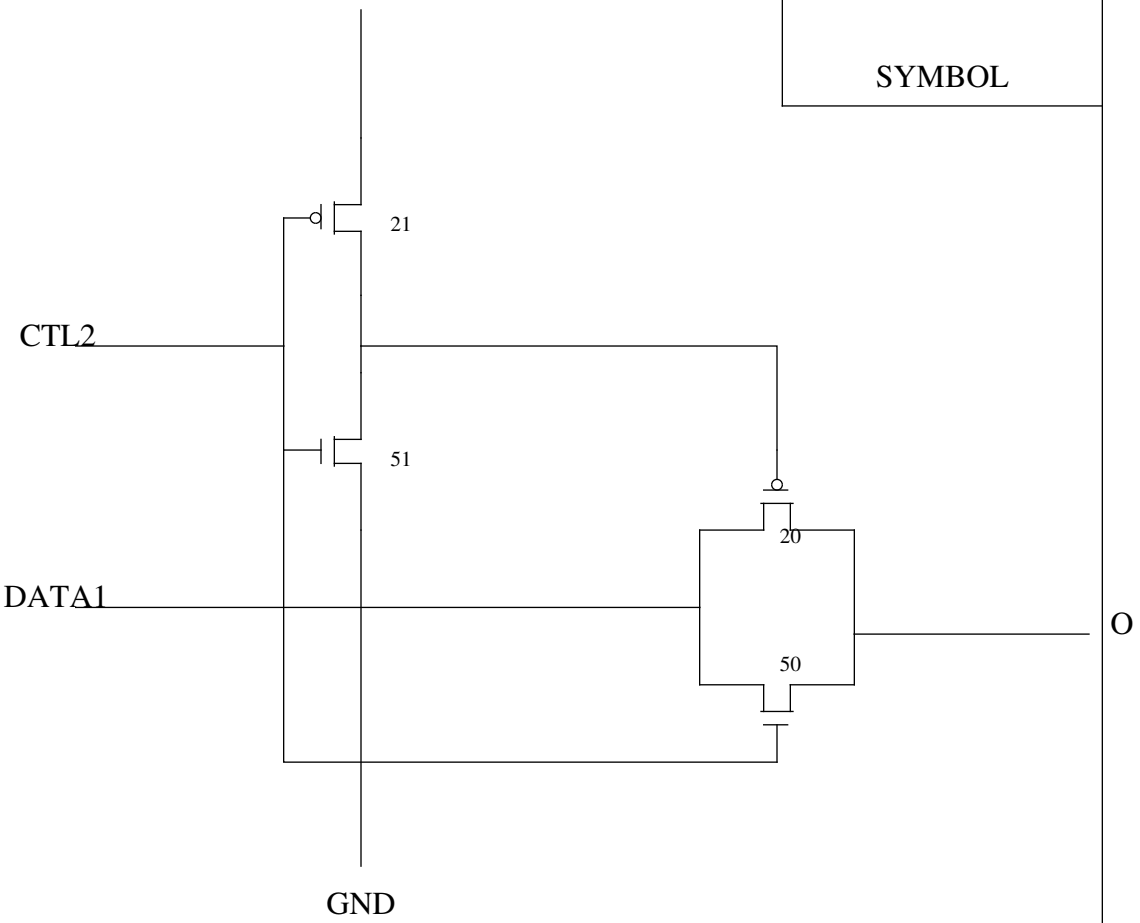


SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	FeedThru	----	----
2	CTL2	21	2
3	FeedThru	----	----
4	DATA1	17	1
5	O	29	0

LOGIC EQUATIONS: O = D * CTL
(Hi-Z at CTL Low)

Truth Table

CTL	D	O
1	0	0
1	1	1
1	-	-
0	0	Z
0	1	Z
0	-	Z