Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**xnsf201** 2_INPUT_STATIC_EX-NOR	DATE: Mar 11,1989 VERSION: dlmV2.0

********** SPICE DECK **********

*** Generated from xnsf201.mag by magic's spice generator
*** technology: scmos
*** timestamp: 605415720
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M8x39 52 25 vdd vdd PMOS W=29.0U L=2.0U
M24x39 vdd 52 120 vdd PMOS W=27.0U L=2.0U
M28x39 120 23 O vdd PMOS W=27.0U L=2.0U
M36x42 O 25 121 vdd PMOS W=26.0U L=2.0U
M44x40 121 54 vdd vdd PMOS W=30.0U L=2.0U
M56x39 vdd 54 23 vdd PMOS W=31.0U L=2.0U
M8x6 52 25 gnd gnd NMOS W=18.0U L=2.0U
M24x13 gnd 25 150 gnd NMOS W=11.0U L=2.0U
M28x13 150 23 O gnd NMOS W=11.0U L=2.0U
M36x6 O 52 151 gnd NMOS W=18.0U L=2.0U
M40x6 151 54 gnd gnd NMOS W=18.0U L=2.0U
M56x4 gnd 54 23 gnd NMOS W=17.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1---O	Pd 0--1	1.27	4.50	2.79	9.90
	Pd 1--0	1.67	4.38	3.67	9.64
	Tr 0--1	2.82	8.87	6.20	19.51
	Tf 1--0	2.57	7.16	5.65	15.75

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1---O	Pd 0--1	3.83	8.03	6.59	13.16
	Pd 1--0	5.01	8.46	8.68	14.08
	Tr 0--1	7.07	15.90	12.60	24.66
	Tf 1--0	5.06	11.51	10.69	19.52

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
51	18	2
50	17	2
53	11	2
55	11	2
52	18	2
54	18	2
21	29	2
20	31	2
23	27	2
22	27	2
25	26	2
24	30	2

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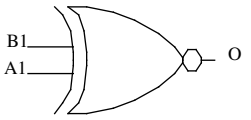
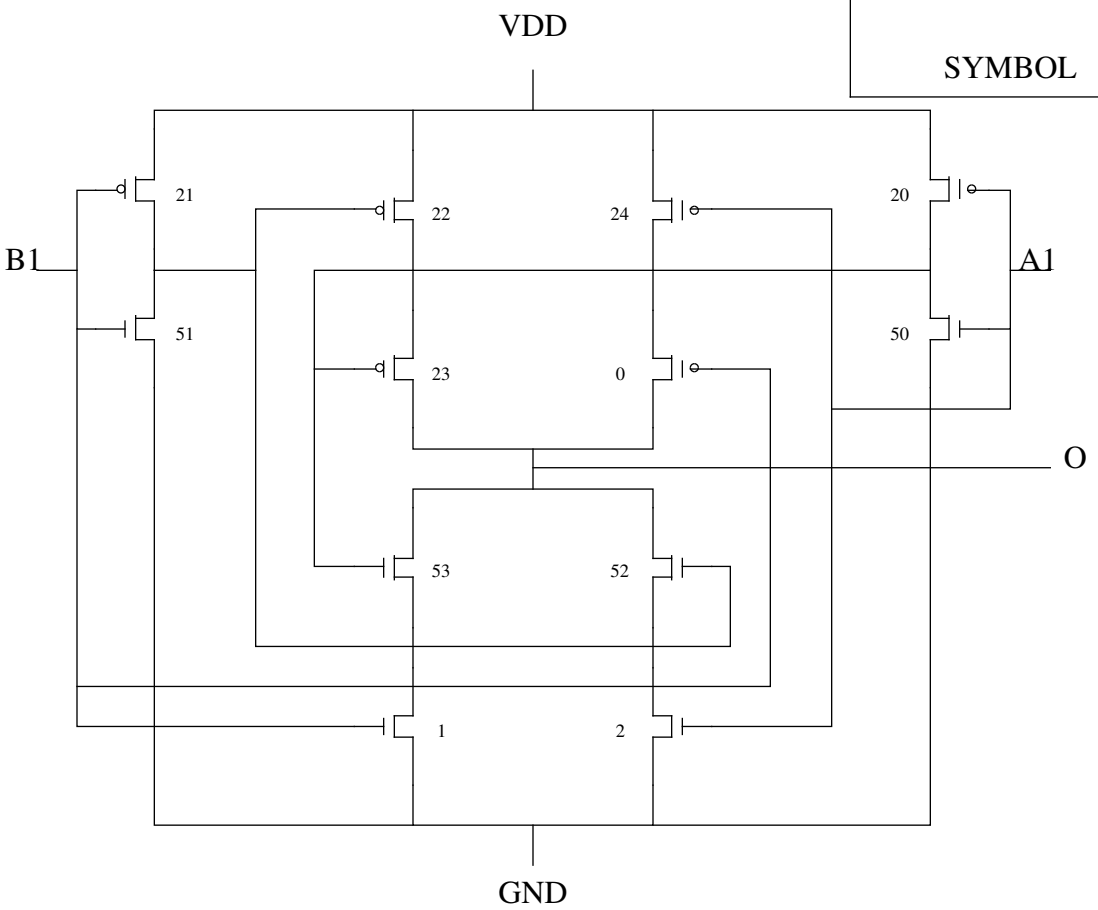


SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	FeedThru	----	----
2	FeedThru	----	----
3	B1	27	1
4	Blocked		----
5	O	52	0
6	FeedThru	----	----
7	A1	27	1
8	FeedThru	----	----

LOGIC EQUATIONS: O = (AB+A'B)';'

Truth Table

A	B	O
0	0	1
1	1	1