Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**xosf201** 2_INPUT_STATIC_EX-OR	DATE: Mar 11,1989 VERSION: dlmV2.0

********** SPICE DECK **********

*** Generated from xosf201.mag by magic's spice generator
*** technology: scmos
*** timestamp: 605415009
*** version: dlm V2.0
*** Capacitance Threshold = 5000000 units
*** Resistance Scale = 1000 units

M8x38 24 23 vdd vdd PMOS W=30.0U L=2.0U
M24x42 vdd 24 120 vdd PMOS W=24.0U L=2.0U
M28x42 120 25 O vdd PMOS W=24.0U L=2.0U
M36x42 O 23 121 vdd PMOS W=26.0U L=2.0U
M44x39 121 22 vdd vdd PMOS W=31.0U L=2.0U
M56x39 vdd 25 22 vdd PMOS W=31.0U L=2.0U
M8x6 24 23 gnd gnd NMOS W=18.0U L=2.0U
M24x8 gnd 24 150 gnd NMOS W=12.0U L=2.0U
M28x8 150 22 O gnd NMOS W=12.0U L=2.0U
M36x8 O 23 151 gnd NMOS W=12.0U L=2.0U
M44x4 151 25 gnd gnd NMOS W=14.0U L=2.0U
M56x4 gnd 25 22 gnd NMOS W=17.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1---O	Pd 0--1	1.13	4.50	2.49	9.90
	Pd 1--0	1.94	4.37	4.27	9.61
	Tr 0--1	2.51	9.48	5.52	20.86
	Tf 1--0	1.50	6.37	3.30	14.01

3-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1---O	Pd 0--1	3.79	8.49	6.71	13.06
	Pd 1--0	5.34	8.77	9.54	14.54
	Tr 0--1	6.23	17.22	11.58	23.70
	Tf 1--0	7.56	12.73	10.93	17.89

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
55	14	2
54	12	2
53	12	2
52	12	2
51	18	2
50	17	2
21	30	2
20	31	2
25	24	2
24	24	2
23	26	2
22	31	2

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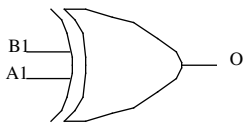
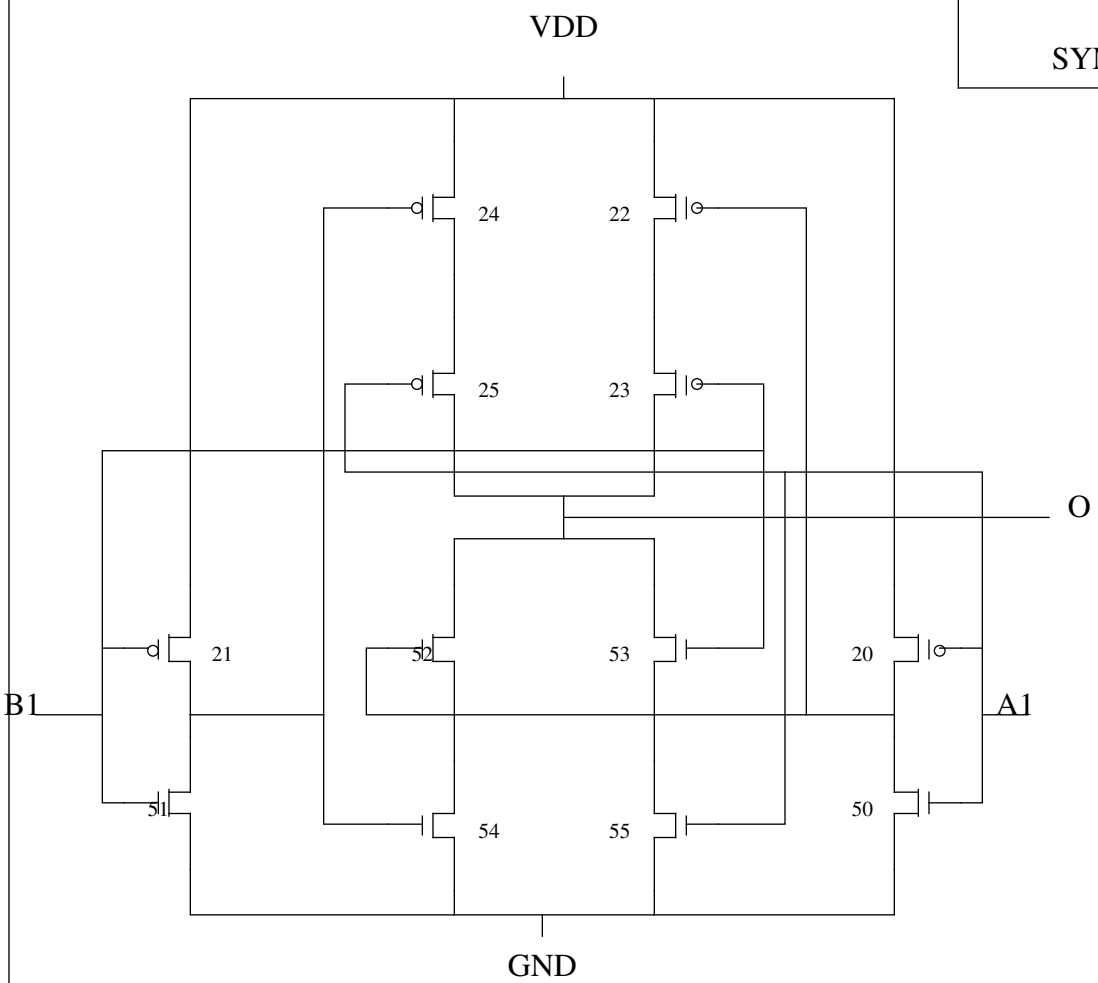


SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	FeedThru	----	----
2	FeedThru	----	----
3	B1	34	1
4	Blocked		----
5	O	51	0
6	FeedThru	----	----
7	A1	26	1
8	FeedThru	----	----

LOGIC EQUATIONS: O = AB+A'B;'

Truth Table

A	B	O
0	1	1
1	0	1