********** SPICE DECK **********

*** Generated from aof2201.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 633228115
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale = 1000 units

M8x39 120 D2 vdd vdd PMOS W=23.0U L=2.0U
M16x39 120 C2 vdd vdd PMOS W=23.0U L=2.0U
M24x39 120 B1 54 vdd PMOS W=23.0U L=2.0U
M32x39 54 A1 120 vdd PMOS W=23.0U L=2.0U
M48x39 O 54 vdd vdd PMOS W=31.0U L=2.0U
M8x12 151 D2 gnd gnd NMOS W=12.0U L=2.0U
M12x12 151 C2 54 gnd NMOS W=12.0U L=2.0U
M24x12 54 B1 150 gnd NMOS W=12.0U L=2.0U
M28x12 150 A1 gnd gnd NMOS W=12.0U L=2.0U
M48x4 O 54 gnd gnd NMOS W=25.0U L=2.0U
C1 54 gnd 89.38fF
C3 D2 gnd 7.10fF
C4 120 gnd 131.58fF
C5 C2 gnd 6.98fF
C6 B1 gnd 7.10fF
C7 A1 gnd 8.07fF
C8 O gnd 99.74fF
C9 151 gnd 7.52fF
C10 150 gnd 7.52fF

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1---O	Pd 0--1	1.11	2.49	3.06	5.66
	Pd 1--0	2.79	3.72	6.85	8.79
	Tr 0--1	1.28	4.99	2.90	8.43
	Tf 1--0	1.19	3.33	2.65	5.42
C2,D2---O	Pd 0--1	1.11	2.49	3.06	5.66
	Pd 1--0	2.79	3.72	6.85	8.79
	Tr 0--1	1.28	4.99	2.90	8.43
	Tf 1--0	1.19	3.33	2.65	5.42

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
54	25	2
53	12	2
51	12	2
50	12	2
52	12	2
24	31	2
20	23	2
21	23	2
22	23	2
23	23	2

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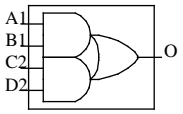
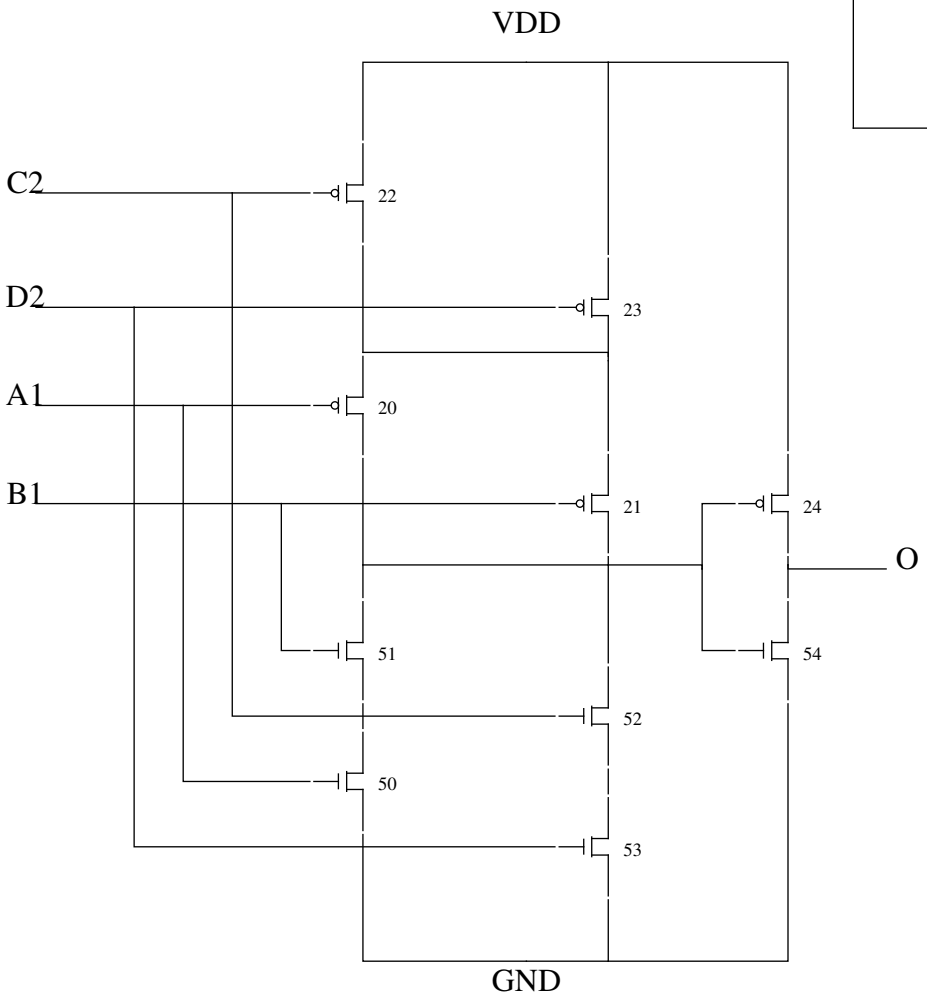
SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**aof2201** 2/2_AND/OR_MUX	DATE: Mar 2,1990 VERSION: dlmV2.2



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	D2	33	2
2	C2	33	2
3	FeedThru	----	----
4	B1	35	1
5	A1	35	1
6	FeedThru	----	----
7	O	33	0

LOGIC EQUATIONS: O = AB + CD

Truth Table

AB	CD	O
-	1	1
1	-	1