********** SPICE DECK **********

*** Generated from blf00001.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 635105990
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale = 1000 units

M8x43 O 50 120 vdd PMOS W=27.0U L=2.0U
M16x43 120 51 vdd vdd PMOS W=19.0U L=2.0U
M24x43 120 52 vdd vdd PMOS W=19.0U L=2.0U
M8x11 O 50 gnd gnd NMOS W=12.0U L=2.0U
M16x4 O 51 150 gnd NMOS W=16.0U L=2.0U
M20x4 150 52 gnd gnd NMOS W=16.0U L=2.0U
C1 50 gnd 7.77fF
C2 O gnd 86.00fF
C3 120 gnd 87.36fF
C5 51 gnd 8.37fF
C6 52 gnd 9.76fF
C7 150 gnd 10.03fF

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	2.17	5.52	5.34	12.99
	Pd 1--0	0.18	2.63	0.62	6.64
	Tr 0--1	3.65	11.67	6.69	21.63
	Tf 1--0	2.79	5.64	5.60	11.88
B2,C2---O	Pd 0--1	2.17	5.52	5.34	12.99
	Pd 1--0	0.19	2.63	1.44	7.20
	Tr 0--1	3.74	11.67	7.30	21.63
	Tf 1--0	3.46	6.91	7.10	13.98

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
51	16	2
52	16	2
50	12	2
21	19	2
20	27	2
22	19	2

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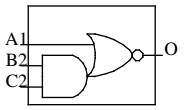
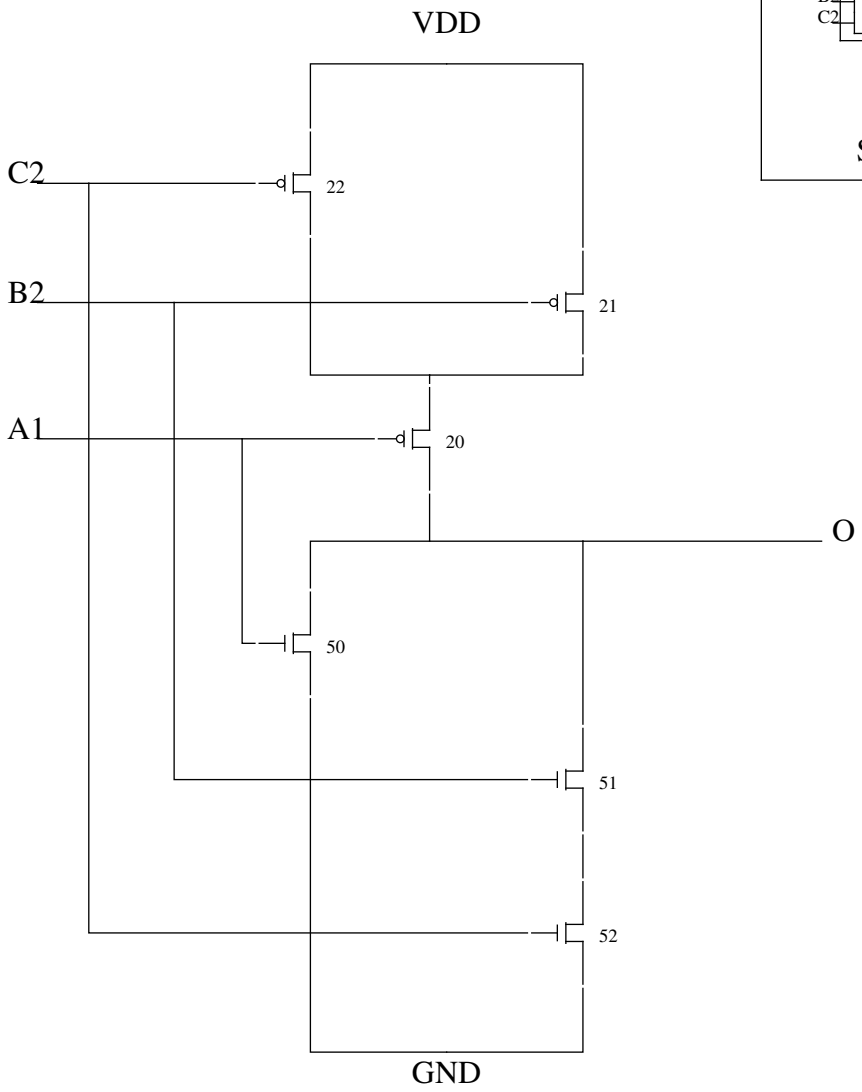
ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**blf00001** 2/1_AND/NOR_MUX	DATE: Mar 6,1990 VERSION: dlmV2.2



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	O	27	0
2	A1	39	1
3	B2	25	2
4	C2	32	2

LOGIC EQUATIONS: O = (A + BC)'

Truth Table

A	BC	O
0	0	1