********** SPICE DECK **********

*** Generated from blf00101.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 633224866
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale = 1000 units

M8x42 O A1 vdd vdd PMOS W=28.0U L=2.0U
M16x39 O 51 120 vdd PMOS W=31.0U L=2.0U
M20x39 120 52 vdd vdd PMOS W=31.0U L=2.0U
M8x4 150 A1 gnd gnd NMOS W=20.0U L=2.0U
M16x15 150 51 O gnd NMOS W=11.0U L=2.0U
M24x15 O 52 150 gnd NMOS W=11.0U L=2.0U
C1 A1 gnd 8.11fF
C2 51 gnd 6.18fF
C3 52 gnd 7.38fF
C5 O gnd 83.79fF
C6 120 gnd 18.35fF
C7 150 gnd 66.50fF

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	1.15	2.92	2.85	7.31
	Pd 1--0	1.63	3.62	4.56	9.77
	Tr 0--1	3.41	6.83	7.56	13.75
	Tf 1--0	3.02	7.00	6.28	14.01
B2,C2---O	Pd 0--1	1.67	4.28	3.83	10.36
	Pd 1--0	1.63	3.62	4.56	9.77
	Tr 0--1	3.41	8.93	7.01	16.81
	Tf 1--0	3.16	7.32	6.89	14.39

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	20	2
52	11	2
51	11	2
22	31	2
21	31	2
20	28	2

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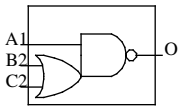
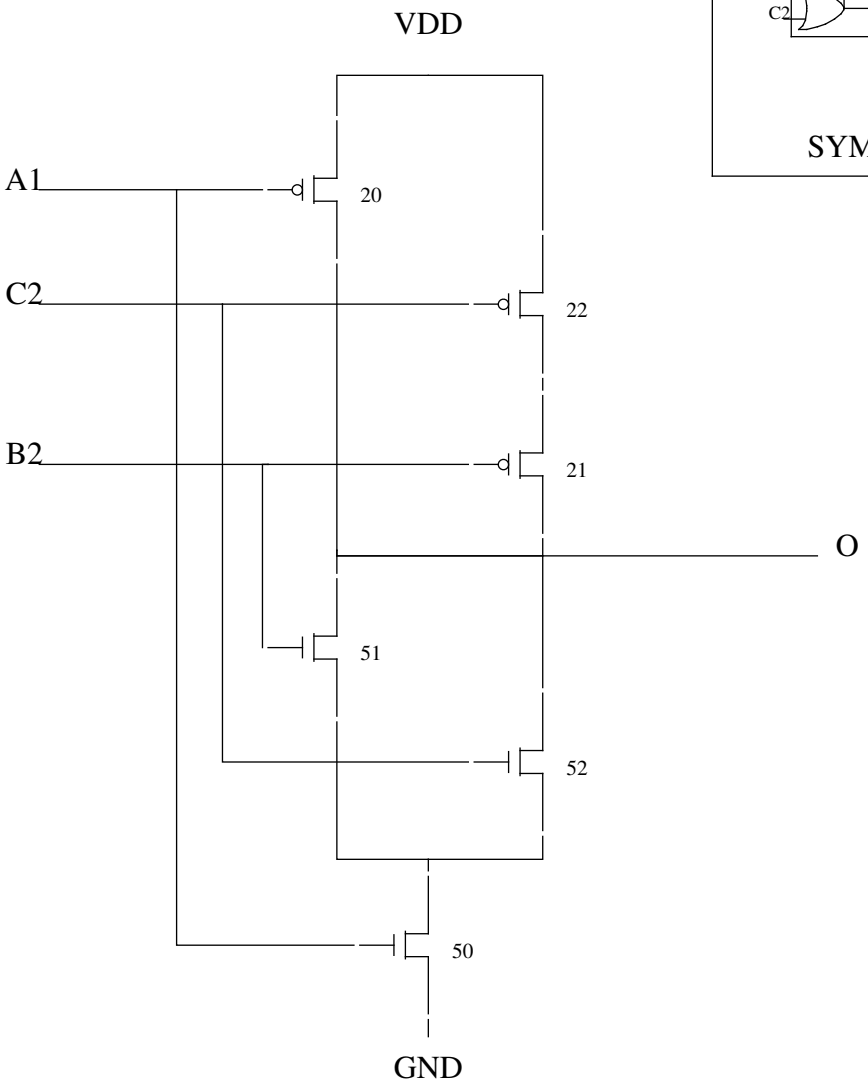
SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**blf00101** 2/1_OR/NAND_MUX	DATE: Mar 4,1990 VERSION: dlmV2.2



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	A1	33	1
2	B2	28	2
3	O	31	0
4	C2	33	2

LOGIC EQUATIONS: O = (A * (B+C))'

Truth Table

A	B	C	O
0	-	-	1
-	0	0	1