********** SPICE DECK **********

*** Generated from buff121.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 636652177
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale = 1000 units

M8x44 23 53 vdd vdd PMOS W=26.0U L=2.0U
M16x44 24 53 vdd vdd PMOS W=26.0U L=2.0U
M27x49 24 23 54 vdd PMOS W=12.0U L=2.0U
M48x42 24 DATA1 vdd vdd PMOS W=16.0U L=2.0U
M56x39 O 24 vdd vdd PMOS W=29.0U L=2.0U
M24x22 24 53 54 gnd NMOS W=12.0U L=2.0U
M8x4 23 53 gnd gnd NMOS W=16.0U L=2.0U
M16x4 54 23 gnd gnd NMOS W=17.0U L=2.0U
M48x16 54 DATA1 gnd gnd NMOS W=13.0U L=2.0U
M56x6 O 54 gnd gnd NMOS W=23.0U L=2.0U
C1 53 gnd 17.37fF
C2 23 gnd 102.00fF
C4 24 gnd 141.77fF
C5 DATA1 gnd 6.21fF
C6 54 gnd 129.47fF
C7 O gnd 94.69fF

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
DATA1---O	Pd 0--1	1.33	2.77	3.48	6.81
	Pd 1--0	2.40	3.28	6.32	8.89
	Tr 0--1	1.13	5.35	2.25	8.45
	Tf 1--0	1.33	3.79	2.43	6.43
EN2---O	Pd 0--1	0.86	2.84	2.41	6.53
	Pd 1--0	0.86	2.33	2.38	5.06
	Tr 0--1	1.31	5.26	3.16	9.08
	Tf 1--0	0.98	2.48	1.84	4.83

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	17	2
52	16	2
51	13	2
54	23	2
53	12	2
20	26	2
22	26	2
24	29	2
23	12	2
21	16	2

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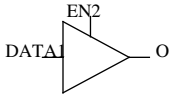
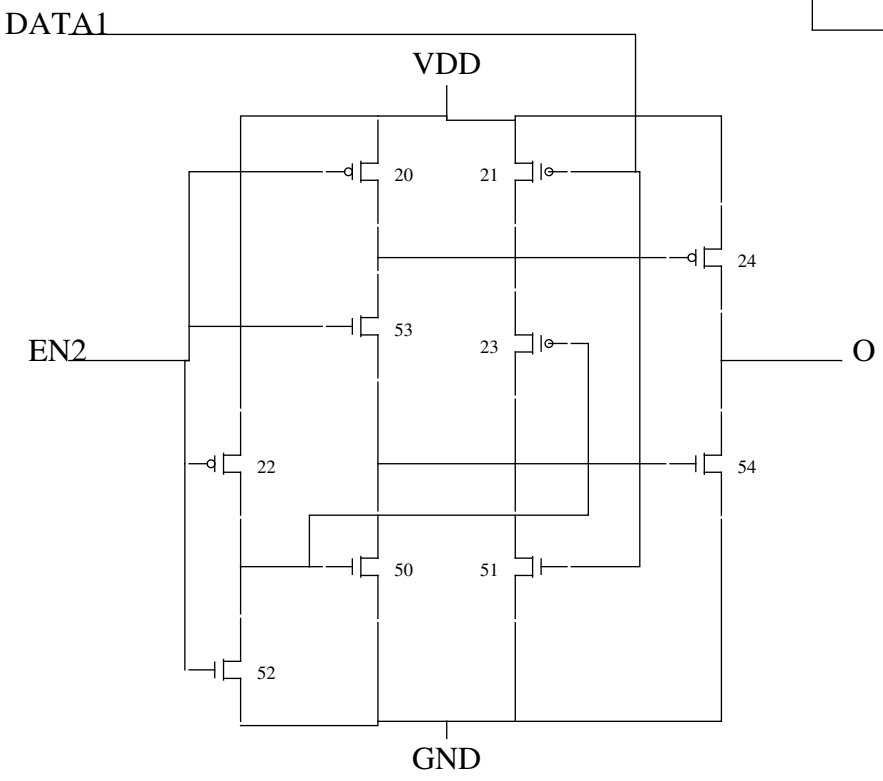
SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**buff121** TRI_STATE_BUFFER	DATE: Mar 6,1990 VERSION: dlmV2.2



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	EN2	36	2
2	FeedThru	----	----
3	FeedThru	----	----
4	FeedThru	----	----
5	FeedThru	----	----
6	DATA1	33	1
7	FeedThru	----	----
8	O	33	0

LOGIC EQUATIONS: O = D * En

Truth Table

EN	D	O
0	-	Z
1	0	0
1	1	1