********** FLIP-FLOP TIMING INFO **********

2u NOMINAL CASE SPECIAL TIMING

Data Setup time = 6.00 ns

Data Hold time = 5.50 ns

Maximum clock rise time > 500 ns

Clock pulse width = 7.50 ns

Reset pulse width = 7.50 ns

Set pulse width = 9.00 ns

2u WORST CASE SPECIAL TIMING

Data Setup time = 5.00 ns

Data Hold time = 5.50 ns

Maximum clock rise time > 500 ns

Clock pulse width = 8.00 ns

Reset pulse width = 8.00 ns

Set pulse width = 9.50 ns

********** SPICE DECK CONTINUED **********

C23 154 gnd 7.45fF
C24 155 gnd 33.87fF
C25 156 gnd 13.11fF

********** SPICE DECK CONTINUED **********

```
M56x4 151 23 152 gnd NMOS W=11.0U L=2.0U
M64x5 152 22 gnd gnd NMOS W=19.0U L=2.0U
M88x8 23 55 153 gnd NMOS W=18.0U L=2.0U
M92x8 153 32 gnd gnd NMOS W=18.0U L=2.0U
M110x8 154 23 gnd gnd NMOS W=11.0U L=2.0U
M114x8 154 21 33 gnd NMOS W=11.0U L=2.0U
M122x8 33 36 Q_b gnd NMOS W=19.0U L=2.0U
M130x5 Q_b 22 155 gnd NMOS W=22.0U L=2.0U
M137x4 155 31 gnd gnd NMOS W=14.0U L=2.0U
M156x4 156 33 gnd gnd NMOS W=23.0U L=2.0U
M160x4 156 32 31 gnd NMOS W=23.0U L=2.0U
C1 vdd 122 5.88fF
C2 vdd 23 5.10fF
C3 21 gnd 102.18fF
C4 64 gnd 8.38fF
C5 20 gnd 10.59fF
C6 36 gnd 94.86fF
C7 22 gnd 31.61fF
C8 55 gnd 126.91fF
C9 32 gnd 28.99fF
C11 120 gnd 18.89fF
C12 122 gnd 117.84fF
C13 23 gnd 98.44fF
C14 121 gnd 7.55fF
C15 123 gnd 18.61fF
C16 33 gnd 89.22fF
C17 Q_b gnd 138.87fF
C18 31 gnd 144.14fF
C19 150 gnd 10.47fF
C20 151 gnd 42.59fF
C21 152 gnd 34.21fF
C22 153 gnd 10.53fF
```

********** SPICE DECK **********

*** Generated from dfbf311.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 613836405
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale = 1000 units

M8x46 36 21 vdd vdd PMOS W=24.0U L=2.0U
M16x46 21 64 vdd vdd PMOS W=24.0U L=2.0U
M36x38 120 20 vdd vdd PMOS W=32.0U L=2.0U
M40x38 120 21 55 vdd PMOS W=32.0U L=2.0U
M50x49 55 36 122 vdd PMOS W=21.0U L=2.0U
M8x4 36 21 gnd gnd NMOS W=18.0U L=2.0U
M16x4 21 64 gnd gnd NMOS W=18.0U L=2.0U
M50x34 55 36 121 vdd PMOS W=11.0U L=2.0U
M54x34 121 23 vdd vdd PMOS W=11.0U L=2.0U
M68x35 122 22 vdd vdd PMOS W=35.0U L=2.0U
M84x46 23 55 vdd vdd PMOS W=24.0U L=2.0U
M92x46 23 32 vdd vdd PMOS W=23.0U L=2.0U
M100x46 123 23 vdd vdd PMOS W=20.0U L=2.0U
M105x46 123 36 33 vdd PMOS W=20.0U L=2.0U
M113x39 33 21 Q_b vdd PMOS W=27.0U L=2.0U
M121x39 Q_b 22 vdd vdd PMOS W=27.0U L=2.0U
M133x39 Q_b 31 vdd vdd PMOS W=27.0U L=2.0U
M148x37 31 33 vdd vdd PMOS W=29.0U L=2.0U
M160x39 31 32 vdd vdd PMOS W=27.0U L=2.0U
M34x4 150 20 gnd gnd NMOS W=17.0U L=2.0U
M38x4 150 36 55 gnd NMOS W=17.0U L=2.0U
M46x4 55 21 151 gnd NMOS W=17.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
CLK2---Q	Pd 0--1	3.20	4.89	7.60	10.61
	Pd 1--0	3.44	4.87	8.97	11.87
	Tr 0--1	1.59	5.58	3.03	9.58
	Tf 1--0	1.45	4.30	2.70	8.36
SET4---Q	Pd 0--1	1.27	2.65	3.22	6.15
	Pd 1--0	N/A	N/A	N/A	N/A
	Tr 0--1	2.83	4.48	5.88	8.33
	Tf 1--0	N/A	N/A	N/A	N/A
RST3---Q	Pd 0--1	N/A	N/A	N/A	N/A
	Pd 1--0	3.88	5.14	8.08	10.62
	Tr 0--1	N/A	N/A	N/A	N/A
	Tf 1--0	1.86	4.02	2.87	8.43
CLK2---Q_B	Pd 0--1	4.09	7.92	10.09	17.36
	Pd 1--0	3.69	7.35	8.60	16.01
	Tr 0--1	1.44	5.49	2.53	10.75
	Tf 1--0	1.20	5.97	2.27	10.59
SET4---Q_B	Pd 0--1	N/A	N/A	N/A	N/A
	Pd 1--0	1.75	4.98	4.32	10.79
	Tr 0--1	N/A	N/A	N/A	N/A
	Tf 1--0	1.55	5.69	2.81	10.26
RST3---Q_B	Pd 0--1	0.84	3.04	2.31	7.24
	Pd 1--0	N/A	N/A	N/A	N/A
	Tr 0--1	2.75	5.52	6.21	11.27
	Tf 1--0	N/A	N/A	N/A	N/A

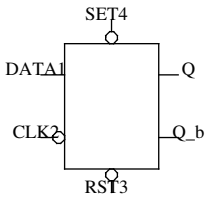
Cell Device Sizes

Transistor	Width (λ)	Length (λ)
61	14	2
52	19	2
60	22	2
57	11	2
53	11	2
54	17	2
51	17	2
50	17	2
64	18	2
65	18	2
56	18	2
55	18	2
58	11	2
59	19	2
63	23	2
62	23	2
29	27	2
31	27	2
30	27	2
28	20	2
25	24	2
27	20	2
26	23	2
34	24	2
35	24	2
21	32	2
20	32	2
33	29	2
32	27	2
24	11	2
23	11	2
22	35	2
36	21	2

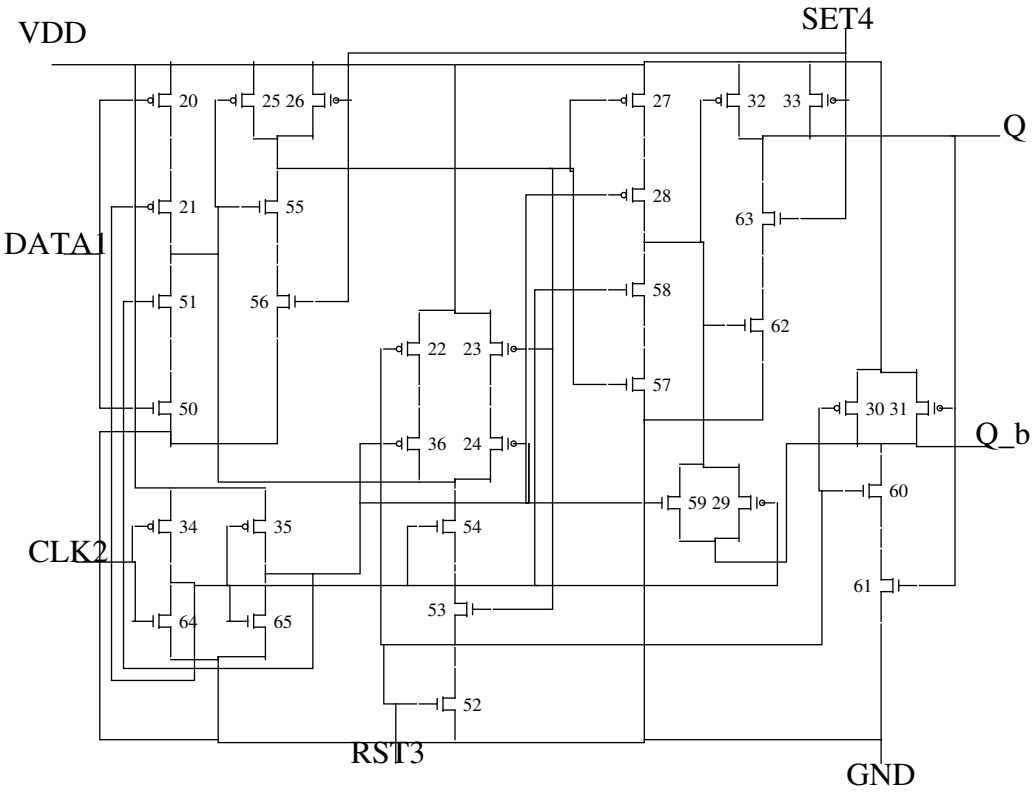
Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**dfbf311** D_FF_W/SET_&_RESET	DATE: Mar 6,1990 VERSION: dlmV2.2



SYMBOL



LOGIC EQUATIONS: Qn = {[(Qn-1*C)+(Dn-1*C)]*R}+S'
Qn'= (NOT Qn) + R'

Truth Table

C	D	R	S	Q	Q'
l2h	-	1	1	Qn-1	Qn-1'
h2l	-	1	1	Dn-1	Dn-1'
-	-	0	1	0	1
-	-	1	0	1	0
-	-	0	0	1	1
-	-	-	0	1	-
-	-	0	-	-	1

TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	FeedThru	----	----
2	FeedThru	----	----
3	CLK2	29	1
4	DATA1	29	0
5	FeedThru	----	----
6	Blocked		----
7	Blocked		----
8	FeedThru	----	----
9	FeedThru	----	----
10	RST3	29	3
11	SET4	29	2
12	FeedThru	----	----
13	FeedThru	----	----
14	FeedThru	----	----
15	FeedThru	----	----
16	FeedThru	----	----
17	FeedThru	----	----
18	Q_b	23	0
19	FeedThru	----	----
20	FeedThru	----	----
21	Q	30	0