********** FLIP-FLOP TIMING INFO **********

2u NOMINAL CASE SPECIAL TIMING

Data Setup time = 11.00 ns

Data Hold time = 6.00 ns

Maximum clock rise time > 500 ns

Clock pulse width = 3.50 ns

2u WORST CASE SPECIAL TIMING

Data Setup time = 10.00 ns

Data Hold time = 5.50 ns

Maximum clock rise time > 500 ns

Clock pulse width = 4.00 ns

********** SPICE DECK CONTINUED **********

```
M80x4 153 61 gnd gnd NMOS W=20.0U L=2.0U
M88x4 61 56 gnd gnd NMOS W=20.0U L=2.0U
C1 27 gnd 135.59fF
C3 22 gnd 59.55fF
C4 28 gnd 6.11fF
C5 57 gnd 94.19fF
C6 30 gnd 109.32fF
C7 51 gnd 8.87fF
C8 61 gnd 97.86fF
C9 56 gnd 100.98fF
C10 120 gnd 7.01fF
C11 121 gnd 6.47fF
C12 122 gnd 10.79fF
C13 123 gnd 17.81fF
C14 150 gnd 9.21fF
C15 151 gnd 7.08fF
C16 152 gnd 7.08fF
C17 153 gnd 11.79fF
```

********** SPICE DECK **********

*** Generated from dfnf311.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 634231247
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale = 1000 units

M8x39 27 28 vdd vdd PMOS W=23.0U L=2.0U
M16x39 57 27 vdd vdd PMOS W=23.0U L=2.0U
M32x44 30 22 vdd vdd PMOS W=22.0U L=2.0U
M40x44 120 51 vdd vdd PMOS W=10.0U L=2.0U
M44x44 120 27 22 vdd PMOS W=10.0U L=2.0U
M52x45 22 30 121 vdd PMOS W=9.0U L=2.0U
M56x45 121 57 vdd vdd PMOS W=9.0U L=2.0U
M8x12 27 28 gnd gnd NMOS W=14.0U L=2.0U
M16x12 57 27 gnd gnd NMOS W=14.0U L=2.0U
M64x45 122 57 vdd vdd PMOS W=17.0U L=2.0U
M68x45 122 30 56 vdd PMOS W=17.0U L=2.0U
M76x39 56 27 123 vdd PMOS W=30.0U L=2.0U
M80x39 123 61 vdd vdd PMOS W=30.0U L=2.0U
M88x39 61 56 vdd vdd PMOS W=31.0U L=2.0U
M32x8 30 22 gnd gnd NMOS W=15.0U L=2.0U
M40x8 150 57 gnd gnd NMOS W=15.0U L=2.0U
M44x8 150 51 22 gnd NMOS W=15.0U L=2.0U
M52x13 22 27 151 gnd NMOS W=11.0U L=2.0U
M56x13 151 30 gnd gnd NMOS W=11.0U L=2.0U
M64x13 152 30 gnd gnd NMOS W=11.0U L=2.0U
M68x13 152 27 56 gnd NMOS W=11.0U L=2.0U
M76x4 56 57 153 gnd NMOS W=20.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
CLK2---Q	Pd 0--1	2.95	2.95	7.16	7.16
	Pd 1--0	3.40	3.40	8.15	8.15
	Tr 0--1	1.10	1.10	2.32	2.32
	Tf 1--0	1.30	1.30	2.32	2.32
CLK2---Q_B	Pd 0--1	3.12	3.12	7.35	7.35
	Pd 1--0	2.33	2.33	6.01	6.01
	Tr 0--1	3.12	3.12	5.97	5.97
	Tf 1--0	2.02	2.02	4.08	4.08

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
51	15	2
50	15	2
52	15	2
57	20	2
58	14	2
59	14	2
53	11	2
60	11	2
54	11	2
55	11	2
61	20	2
56	20	2
21	10	2
20	10	2
22	22	2
23	9	2
24	17	2
28	23	2
29	23	2
27	30	2
25	17	2
30	9	2
31	30	2
26	31	2

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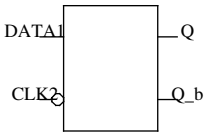
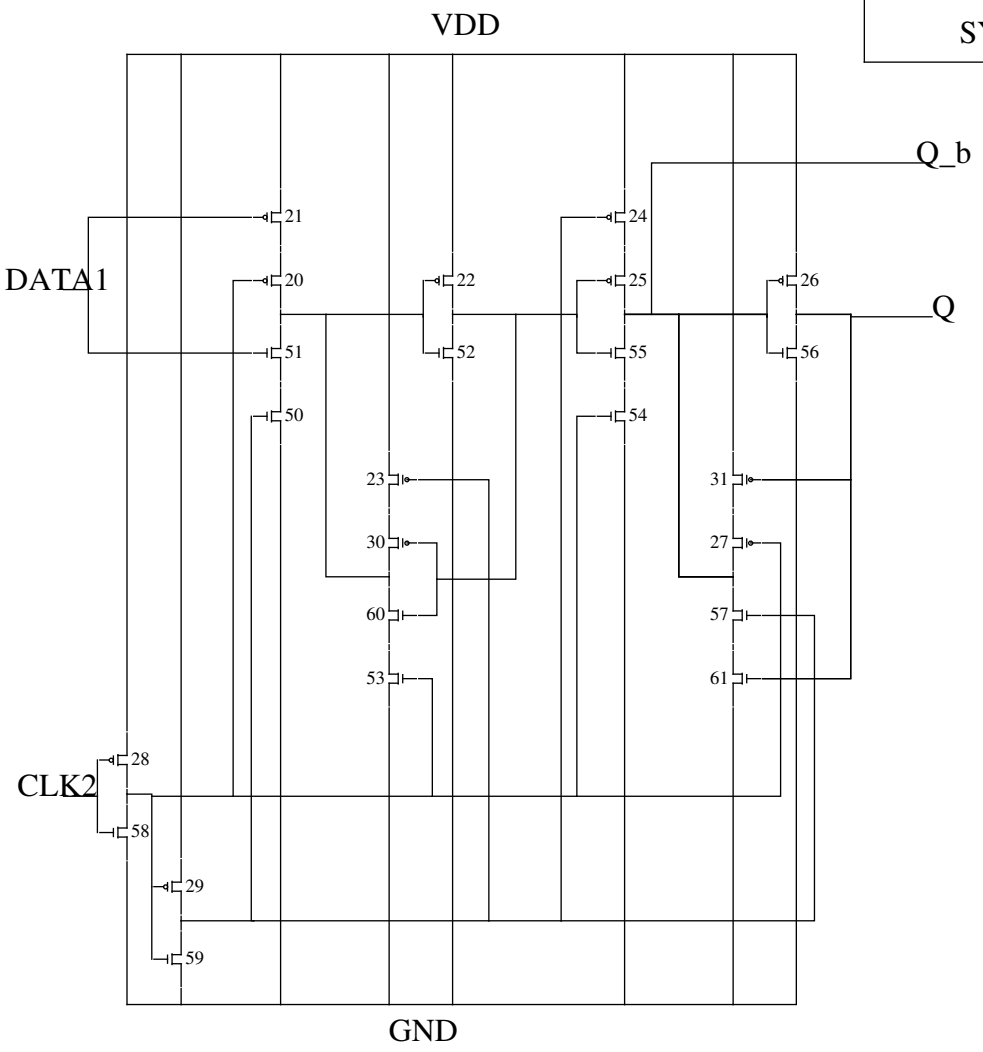
ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**dfnf311** D_FF_W/Q_&_Q'	DATE: Mar 7,1990 VERSION: dlmV2.2



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	CLK2	34	1
2	FeedThru	----	----
3	FeedThru	----	----
4	FeedThru	----	----
5	DATA1	46	0
6	Blocked		----
7	FeedThru	----	----
8	FeedThru	----	----
9	FeedThru	----	----
10	Q_b	33	0
11	FeedThru	----	----
12	Q	26	0

LOGIC EQUATIONS: Q = (Qn-1 * C) + (Dn-1 * C')
Q' = (NOT Q)

Truth Table

C	D	Q	Q'
h2l	-	D	D'
l2h	-	Qn-1	Qn-1'