********** FLIP-FLOP TIMING INFO **********

2u NOMINAL CASE SPECIAL TIMING

Data Setup time = 7.50 ns

Data Hold time = 6.00 ns

Maximum clock rise time > 500 ns

Clock pulse width = 5.50 ns

Reset pulse width = 2.50 ns

2u WORST CASE SPECIAL TIMING

Data Setup time = 7.00 ns

Data Hold time = 6.00 ns

Maximum clock rise time > 500ns

Clock pulse width = 6.00 ns

Reset pulse width = 2.50 ns

********** SPICE DECK CONTINUED **********

```
M78x8 24 52 gnd gnd NMOS W=15.0U L=2.0U
M99x8 153 24 gnd gnd NMOS W=13.0U L=2.0U
M103x8 153 65 154 gnd NMOS W=13.0U L=2.0U
M107x8 154 57 58 gnd NMOS W=13.0U L=2.0U
M115x8 58 27 155 gnd NMOS W=17.0U L=2.0U
M119x8 155 Q 156 gnd NMOS W=17.0U L=2.0U
M123x8 156 65 gnd gnd NMOS W=17.0U L=2.0U
M144x4 Q 58 gnd gnd NMOS W=21.0U L=2.0U
M160x6 Q_b Q gnd gnd NMOS W=12.0U L=2.0U
C1 CLK2 gnd 6.27fF
C2 57 gnd 119.08fF
C3 DATA1 gnd 9.68fF
C4 27 gnd 119.38fF
C5 Q gnd 110.53fF
C6 65 gnd 35.22fF
C7 58 gnd 132.16fF
C9 120 gnd 15.65fF
C10 52 gnd 94.35fF
C11 24 gnd 96.61fF
C12 121 gnd 76.98fF
C13 123 gnd 12.95fF
C14 124 gnd 17.81fF
C15 Q_b gnd 86.57fF
C16 150 gnd 11.35fF
C17 152 gnd 9.21fF
C18 151 gnd 9.21fF
C19 153 gnd 8.33fF
C20 154 gnd 8.33fF
C21 155 gnd 10.09fF
C22 156 gnd 10.09fF
```

********** SPICE DECK **********

*** Generated from dfrf311.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 628905226
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale = 1000 units

M8x41 57 CLK2 vdd vdd PMOS W=29.0U L=2.0U
M16x41 27 57 vdd vdd PMOS W=29.0U L=2.0U
M34x44 120 DATA1 vdd vdd PMOS W=26.0U L=2.0U
M38x44 120 57 52 vdd PMOS W=26.0U L=2.0U
M46x44 52 27 121 vdd PMOS W=22.0U L=2.0U
M54x44 121 24 vdd vdd PMOS W=22.0U L=2.0U
M62x44 121 65 vdd vdd PMOS W=22.0U L=2.0U
M76x44 24 52 vdd vdd PMOS W=22.0U L=2.0U
M8x4 57 CLK2 gnd gnd NMOS W=24.0U L=2.0U
M16x4 27 57 gnd gnd NMOS W=24.0U L=2.0U
M96x45 123 24 vdd vdd PMOS W=21.0U L=2.0U
M100x45 123 27 58 vdd PMOS W=21.0U L=2.0U
M114x40 124 57 vdd vdd PMOS W=30.0U L=2.0U
M118x40 124 Q 58 vdd PMOS W=30.0U L=2.0U
M126x39 58 65 vdd vdd PMOS W=31.0U L=2.0U
M144x39 Q 58 vdd vdd PMOS W=31.0U L=2.0U
M160x41 Q_b Q vdd vdd PMOS W=29.0U L=2.0U
M42x4 150 DATA1 gnd gnd NMOS W=19.0U L=2.0U
M46x4 150 27 52 gnd NMOS W=19.0U L=2.0U
M54x8 52 65 152 gnd NMOS W=15.0U L=2.0U
M58x8 152 24 151 gnd NMOS W=15.0U L=2.0U
M62x8 151 57 gnd gnd NMOS W=15.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
CLK2---Q	Pd 0--1	3.87	5.45	8.84	11.96
	Pd 1--0	3.54	4.74	8.49	10.68
	Tr 0--1	1.58	4.51	3.23	9.42
	Tf 1--0	1.50	3.24	2.73	6.24
RST3---Q	Pd 0--1	N/A	N/A	N/A	N/A
	Pd 1--0	1.43	2.41	3.06	4.65
	Tr 0--1	N/A	N/A	N/A	N/A
	Tf 1--0	1.90	3.00	3.05	5.77
CLK2---Q_B	Pd 0--1	3.81	7.14	9.00	15.10
	Pd 1--0	4.17	7.97	9.44	16.70
	Tr 0--1	0.98	4.59	1.80	8.96
	Tf 1--0	0.69	4.51	1.50	8.64
RST3---Q_B	Pd 0--1	1.70	4.62	3.81	8.91
	Pd 1--0	N/A	N/A	N/A	N/A
	Tr 0--1	0.88	4.50	1.48	8.59
	Tf 1--0	N/A	N/A	N/A	N/A

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
64	12	2
62	24	2
63	24	2
51	19	2
50	19	2
55	15	2
54	15	2
53	15	2
52	15	2
56	13	2
61	17	2
59	17	2
58	21	2
57	13	2
60	17	2
65	13	2
34	29	2
33	29	2
32	29	2
20	26	2
21	26	2
25	22	2
23	22	2
22	22	2
27	21	2
26	21	2
31	30	2
29	30	2
30	31	2
28	31	2
24	22	2

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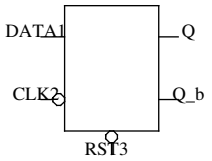
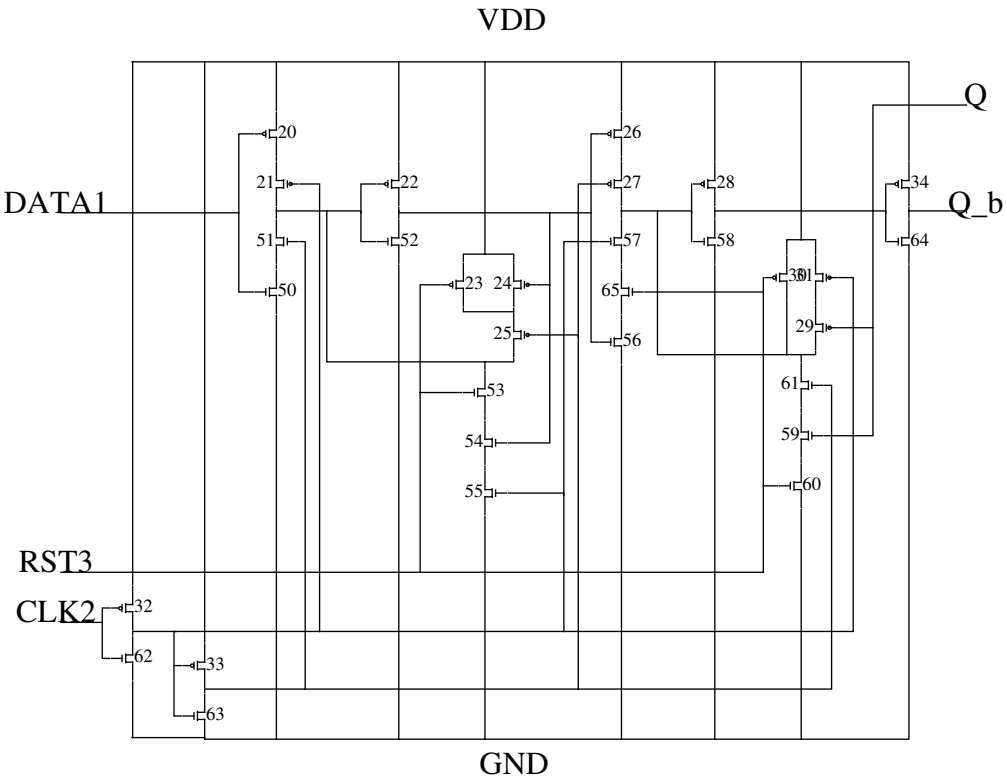
SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**dfrf311** D_FF_W/Q_Q'_&_ASY_RST	DATE: Mar 7,1990 VERSION: dlmV2.2



SYMBOL



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LOGIC EQUATIONS: Q = [(Qn-1 * C) + (Dn-1 * C')]*R
Q'= (NOT Q)

Truth Table

C	D	R	Q	Q'
l2h	-	1	Qn-1	Qn-1'
h2l	-	1	D	D'
-	-	0	0	1
-	-	1	-	-

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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	FeedThru	----	----
2	CLK2	24	1
3	FeedThru	----	----
4	DATA1	26	0
5	Blocked		----
6	Blocked		----
7	Blocked		----
8	FeedThru	----	----
9	FeedThru	----	----
10	Blocked		----
11	FeedThru	----	----
12	Blocked		----
13	Blocked		----
14	FeedThru	----	----
15	FeedThru	----	----
16	Blocked		----
17	RST3	27	2
18	FeedThru	----	----
19	Q	31	0
20	FeedThru	----	----
21	Q_b	33	0