********** SPICE DECK CONTINUED **********

```
M84x4 154 26 gnd gnd NMOS W=21.0U L=2.0U
M92x7 154 B1 gnd gnd NMOS W=21.0U L=2.0U
M100x8 154 CIN2 55 gnd NMOS W=20.0U L=2.0U
M108x7 55 B1 152 gnd NMOS W=21.0U L=2.0U
M112x7 152 26 gnd gnd NMOS W=21.0U L=2.0U
M128x4 CO 55 gnd gnd NMOS W=24.0U L=2.0U
C1 55 vdd 6.04fF
C2 123 vdd 6.06fF
C3 63 gnd 90.83fF
C4 SUM gnd 76.77fF
C6 26 gnd 37.81fF
C7 B1 gnd 33.76fF
C8 CIN2 gnd 25.75fF
C9 120 gnd 16.73fF
C10 121 gnd 16.73fF
C11 55 gnd 108.30fF
C12 123 gnd 102.19fF
C13 124 gnd 103.68fF
C14 122 gnd 18.35fF
C15 150 gnd 6.64fF
C16 151 gnd 6.64fF
C17 153 gnd 74.03fF
C18 CO gnd 93.53fF
C19 154 gnd 70.95fF
C20 152 gnd 11.95fF
```

********** SPICE DECK **********

*** Generated from faf001.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 628905226
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale = 1000 units

M12x41 SUM 63 vdd vdd PMOS W=29.0U L=2.0U
M20x41 120 26 vdd vdd PMOS W=28.0U L=2.0U
M24x41 120 B1 121 vdd PMOS W=28.0U L=2.0U
M28x41 121 CIN2 63 vdd PMOS W=28.0U L=2.0U
M36x41 63 55 123 vdd PMOS W=25.0U L=2.0U
M44x41 123 CIN2 vdd vdd PMOS W=28.0U L=2.0U
M60x41 123 B1 vdd vdd PMOS W=29.0U L=2.0U
M68x43 123 26 vdd vdd PMOS W=27.0U L=2.0U
M8x13 SUM 63 gnd gnd NMOS W=16.0U L=2.0U
M84x38 124 26 vdd vdd PMOS W=31.0U L=2.0U
M92x38 124 B1 vdd vdd PMOS W=29.0U L=2.0U
M100x38 124 CIN2 55 vdd PMOS W=28.0U L=2.0U
M108x38 55 B1 122 vdd PMOS W=31.0U L=2.0U
M112x38 122 26 vdd vdd PMOS W=31.0U L=2.0U
M20x13 150 26 gnd gnd NMOS W=10.0U L=2.0U
M24x13 150 B1 151 gnd NMOS W=10.0U L=2.0U
M28x13 151 CIN2 63 gnd NMOS W=10.0U L=2.0U
M36x12 63 55 153 gnd NMOS W=19.0U L=2.0U
M44x12 153 CIN2 gnd gnd NMOS W=19.0U L=2.0U
M128x39 CO 55 vdd vdd PMOS W=31.0U L=2.0U
M60x4 153 B1 gnd gnd NMOS W=24.0U L=2.0U
M68x4 153 26 gnd gnd NMOS W=16.0U L=2.0U

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1---SUM	Pd 0--1	3.33	4.71	7.86	10.24
	Pd 1--0	2.96	4.21	6.97	9.81
	Tr 0--1	1.58	5.94	2.95	9.44
	Tf 1--0	1.52	4.50	3.03	7.19
CIN2---SUM	Pd 0--1	3.21	4.73	7.70	11.05
	Pd 1--0	2.91	4.15	7.20	10.03
	Tr 0--1	1.67	5.79	2.63	9.45
	Tf 1--0	1.46	4.53	2.69	7.20
A1,B1---CO	Pd 0--1	1.61	3.45	3.88	6.81
	Pd 1--0	2.51	3.58	6.21	8.26
	Tr 0--1	1.42	4.89	2.81	8.70
	Tf 1--0	1.39	3.06	2.39	6.04
CIN2---CO	Pd 0--1	1.25	2.69	3.30	6.09
	Pd 1--0	2.21	3.31	5.67	7.71
	Tr 0--1	1.13	4.91	2.14	8.64
	Tf 1--0	1.55	3.22	2.74	5.89

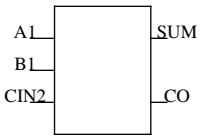
Cell Device Sizes

Transistor	Width (λ)	Length (λ)
58	19	2
59	19	2
62	10	2
61	10	2
60	10	2
63	16	2
57	24	2
56	16	2
52	21	2
53	21	2
54	20	2
50	21	2
51	21	2
55	24	2
33	29	2
30	28	2
31	28	2
32	28	2
29	25	2
28	28	2
27	29	2
20	31	2
21	31	2
23	29	2
22	31	2
24	28	2
26	27	2
25	31	2

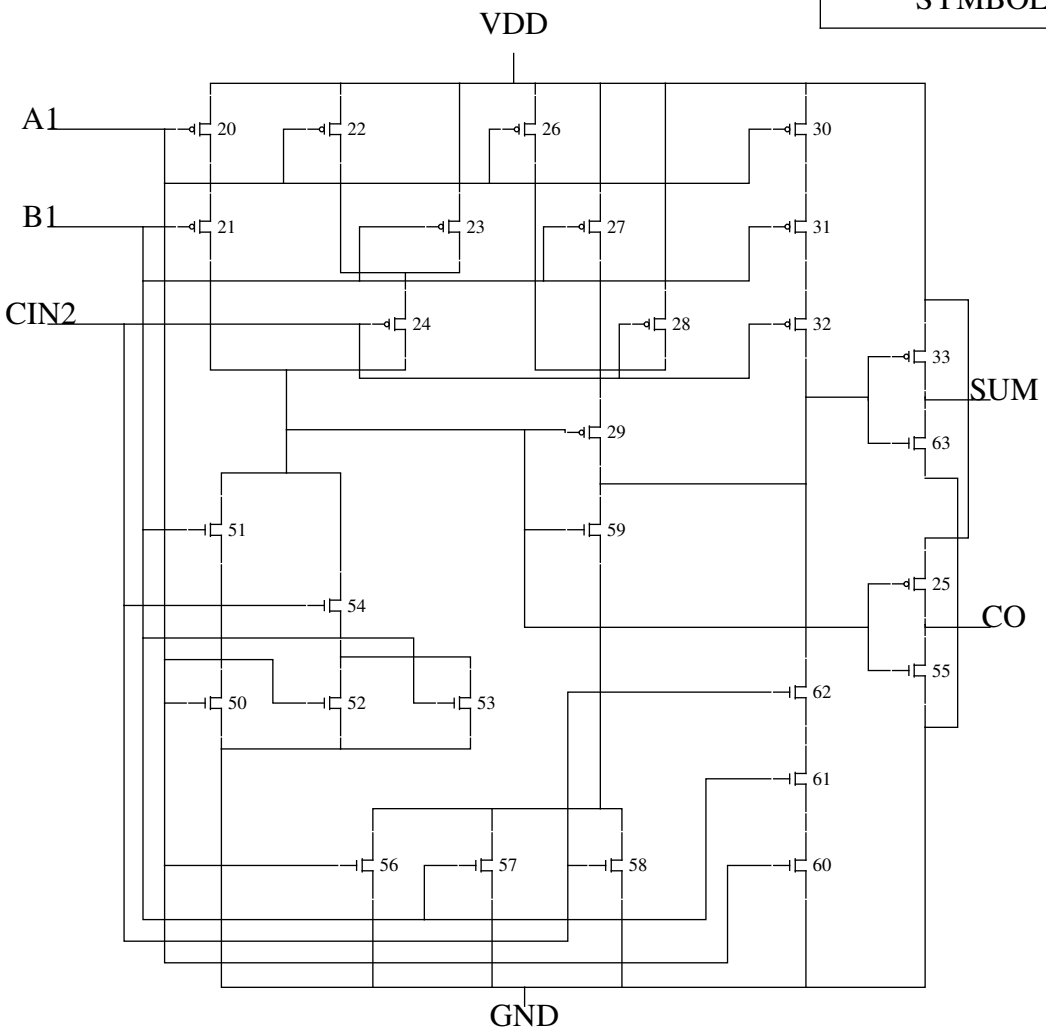
Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**faf001** FULL_ADDER	DATE: Mar 6,1990 VERSION: dlmV2.2



SYMBOL



Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**faf001** FULL_ADDER	DATE: Mar 6,1990 VERSION: dlmV2.2

TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	SUM	44	0
2	FeedThru	----	----
3	FeedThru	----	----
4	FeedThru	----	----
5	FeedThru	----	----
6	FeedThru	----	----
7	FeedThru	----	----
8	FeedThru	----	----
9	CIN2	36	2
10	A1	23	1
11	B1	30	1
12	FeedThru	----	----
13	FeedThru	----	----
14	FeedThru	----	----
15	FeedThru	----	----
16	FeedThru	----	----
17	CO	32	0

LOGIC EQUATIONS: S = A xor B xor C
CO = AB xor AC xor BC

Truth Table

A	B	C	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1