********** SPICE DECK **********

*** Generated from invf100.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 628905226
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale = 1000 units

M4x46 O 20 vdd vdd PMOS W=4.0U L=2.0U
M5x20 O 20 gnd gnd NMOS W=3.0U L=4.0U
C2 20 gnd 10.64fF
C3 O gnd 24.84fF

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	0.68	10.47	1.81	24.02
	Pd 1--0	0.89	10.61	2.76	26.36
	Tr 0--1	2.29	23.72	6.01	49.71
	Tf 1--0	2.22	19.90	5.58	47.57

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	3	4
20	4	2

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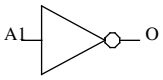
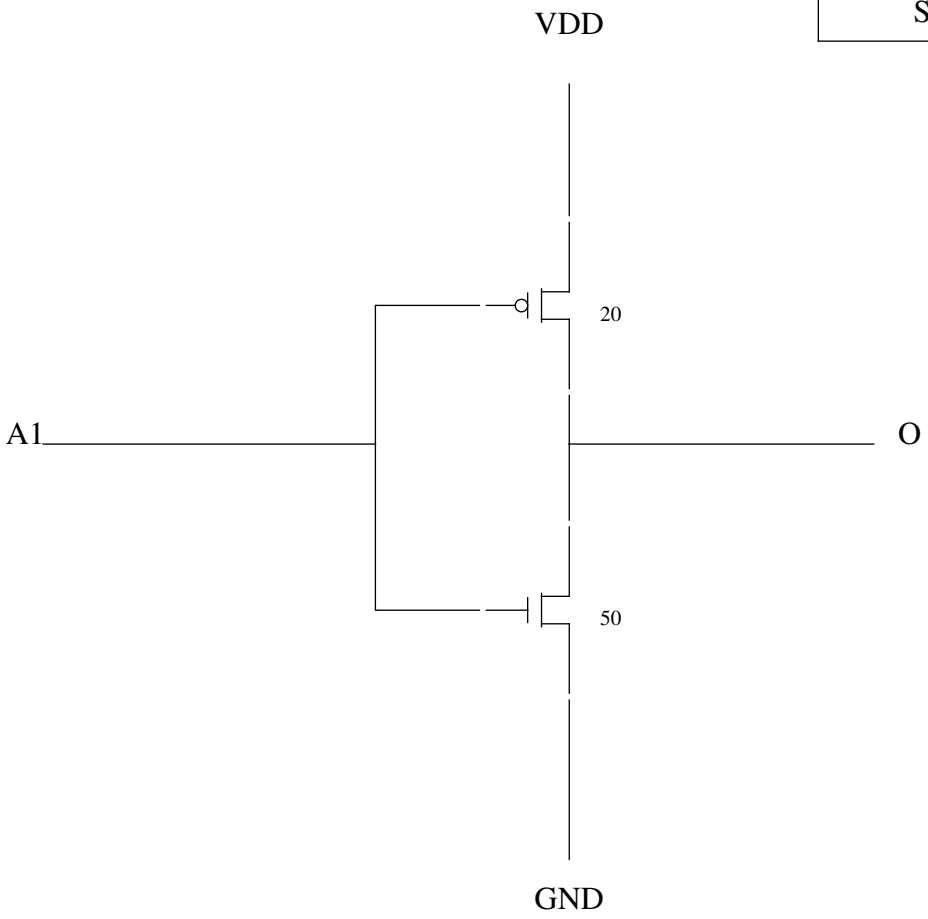
SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**invf100** HI_Z_INVERTER	DATE: Mar 6,1990 VERSION: dlmV2.2



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	O	33	0
2	A1	33	1

LOGIC EQUATIONS: O = A'

Truth Table

A	O
0	1