********** SPICE DECK **********

*** Generated from invf103.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 628905226
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale = 1000 units

M8x45 O A1 vdd vdd PMOS W=25.0U L=2.0U
M16x45 O A1 vdd vdd PMOS W=25.0U L=2.0U
M24x45 O A1 vdd vdd PMOS W=25.0U L=2.0U
M8x12 O A1 gnd gnd NMOS W=12.0U L=2.0U
M16x12 O A1 gnd gnd NMOS W=12.0U L=2.0U
M24x12 O A1 gnd gnd NMOS W=12.0U L=2.0U
C1 A1 gnd 22.36fF
C2 O gnd 144.09fF

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
IN---OUT	Pd 0--1	0.62	1.48	1.15	3.78
	Pd 1--0	0.03	0.86	0.59	3.05
	Tr 0--1	2.13	3.84	4.97	7.98
	Tf 1--0	2.15	3.04	4.46	6.95

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	36	2
20	75	2

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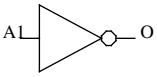
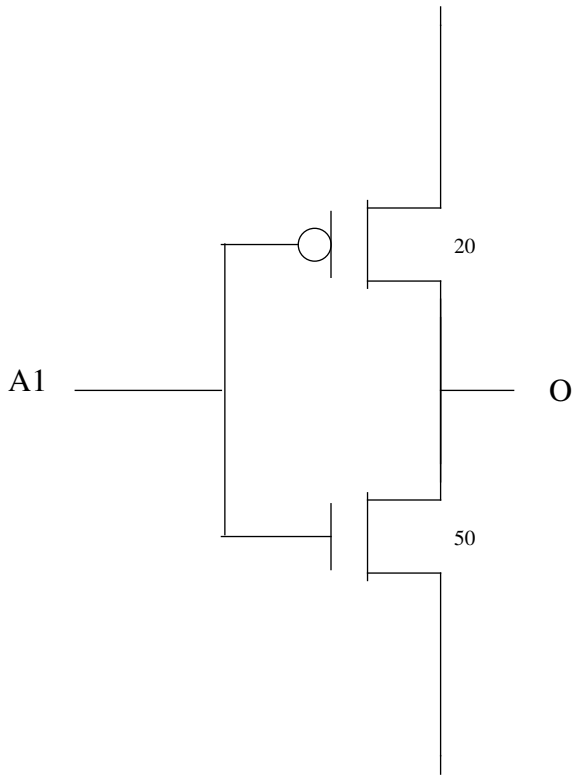
SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**invf103** 3X_INVERTING_BUFFER	DATE: Mar 3,1990 VERSION: dlmV2.2



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	O	31	O
2	A1	31	I
3	FeedThru	----	----
4	FeedThru	----	----

LOGIC EQUATIONS: O = A'

Truth Table

A	O
0	1