********** SPICE DECK **********

*** Generated from invf104.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 628905226
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale = 1000 units

M8x44 O 50 vdd vdd PMOS W=26.0U L=2.0U
M16x40 O 50 vdd vdd PMOS W=30.0U L=2.0U
M24x40 O 50 vdd vdd PMOS W=30.0U L=2.0U
M32x44 O 50 vdd vdd PMOS W=26.0U L=2.0U
M8x12 O 50 gnd gnd NMOS W=11.0U L=2.0U
M16x12 O 50 gnd gnd NMOS W=11.0U L=2.0U
M24x12 O 50 gnd gnd NMOS W=11.0U L=2.0U
M32x12 O 50 gnd gnd NMOS W=11.0U L=2.0U
C1 vdd OUT 5.64fF
C2 50 gnd 25.50fF
C4 O gnd 153.75fF

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	0.41	0.91	0.66	2.65
	Pd 1--0	0.23	0.79	0.92	2.96
	Tr 0--1	2.20	3.29	4.71	7.20
	Tf 1--0	2.01	2.75	4.36	6.46

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	44	2
20	60	2

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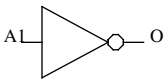
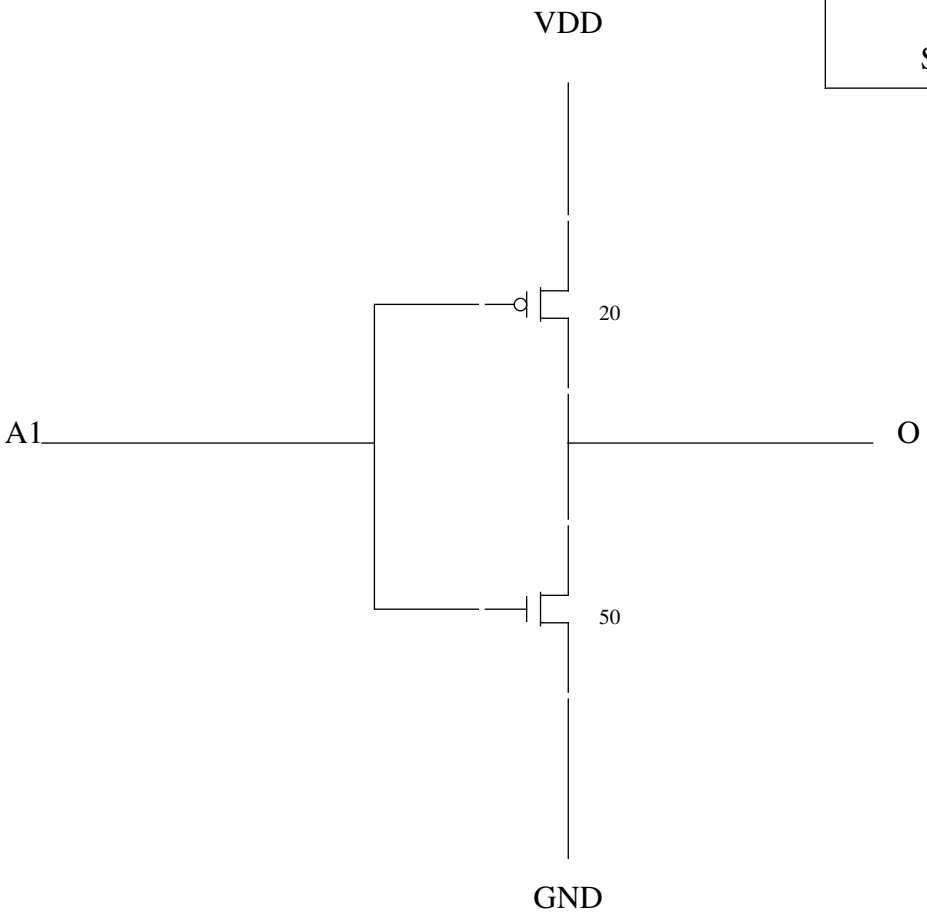
SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**invf104** 4X_INVERTING_BUFFER	DATE: Mar 6,1990 VERSION: dlmV2.2



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	FeedThru	----	----
2	O	33	0
3	FeedThru	----	----
4	A1	28	1
5	FeedThru	----	----

LOGIC EQUATIONS: O = A'

Truth Table

A	O
0	1