Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**invf121** TRI_STATE_INVERTER	DATE: Mar 5,1990 VERSION: dlmV2.2

```
**************** SPICE DECK ********************

*** Generated from invf121.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 632957678
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale      = 1000 units


M8x33 120 22 vdd vdd PMOS W=32.0U L=2.0U
M12x33 120 50 O vdd PMOS W=32.0U L=2.0U
M20x33 O 50 121 vdd PMOS W=32.0U L=2.0U
M24x33 121 22 vdd vdd PMOS W=32.0U L=2.0U
M36x39 52 22 vdd vdd PMOS W=15.0U L=2.0U
M8x8 150 52 gnd gnd NMOS W=14.0U L=2.0U
M12x8 150 50 O gnd NMOS W=14.0U L=2.0U
M20x8 O 50 151 gnd NMOS W=14.0U L=2.0U
M24x8 151 52 gnd gnd NMOS W=14.0U L=2.0U
M36x15 52 22 gnd gnd NMOS W=8.0U L=2.0U
C2 22 gnd 21.73fF
C3 50 gnd 14.14fF
C4 120 gnd 18.89fF
C5 O gnd 85.84fF
C6 121 gnd 18.89fF
C7 52 gnd 62.19fF
C8 150 gnd 8.77fF
C9 151 gnd 8.77fF
```

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	0.71	2.23	1.30	5.62
	Pd 1--0	0.20	1.64	0.93	5.05
	Tr 0--1	2.49	5.61	5.66	11.15
	Tf 1--0	2.33	4.40	4.94	9.84
ENB---O	Pd 0--1	N/A	N/A	N/A	N/A
	Pd 1--0	0.99	2.31	2.16	4.89
	Tr 0--1	N/A	N/A	N/A	N/A
	Tf 1--0	1.13	3.49	2.89	6.68

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
51	8	2
52	28	2
50	28	2
20	64	2
21	15	2
22	64	2

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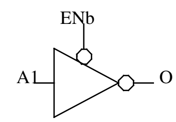
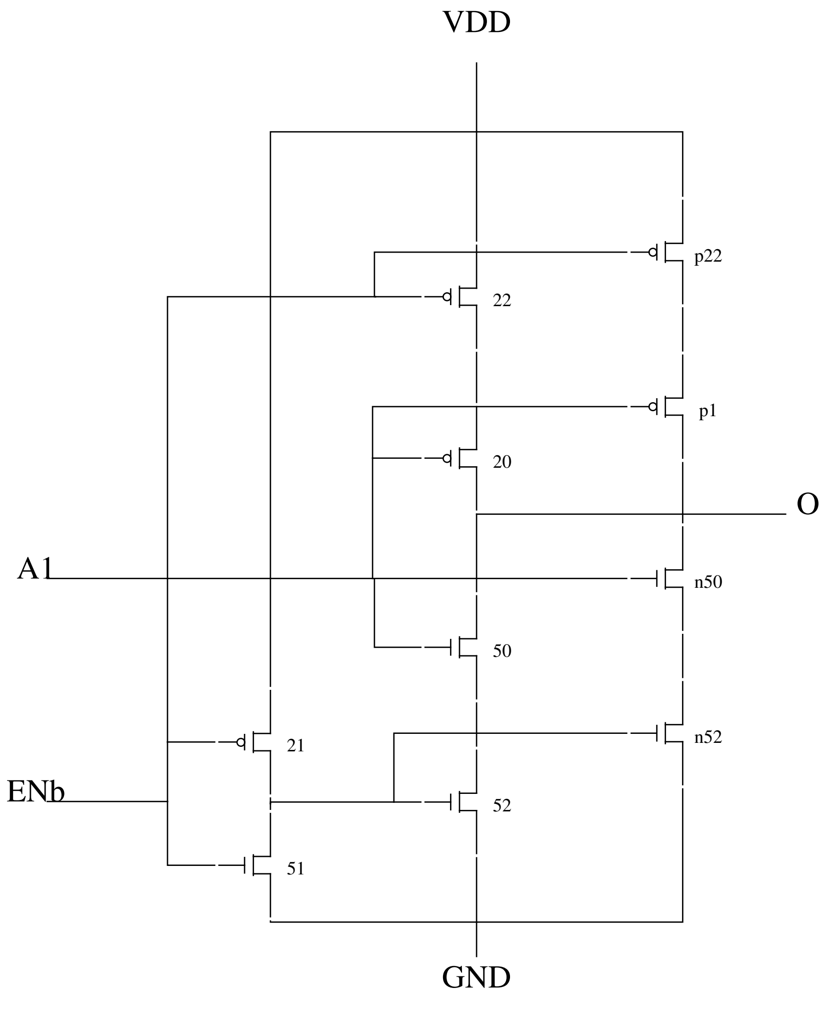


SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	A1	0	1
2	FeedThru	----	----
3	O	0	0
4	FeedThru	----	----
5	FeedThru	----	----
6	ENb	0	2

LOGIC EQUATIONS: O = D * ENb'

Truth Table

D	ENb	O
1	0	1