********** SPICE DECK **********

*** Generated from invf201.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 628905226
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale = 1000 units

M8x41 O1 50 vdd vdd PMOS W=29.0U L=2.0U
M24x41 O2 51 vdd vdd PMOS W=29.0U L=2.0U
M8x13 O1 50 gnd gnd NMOS W=13.0U L=2.0U
M24x13 O2 51 gnd gnd NMOS W=13.0U L=2.0U
C1 50 gnd 6.74fF
C2 51 gnd 6.74fF
C3 O1 gnd 77.62fF
C5 O2 gnd 77.62fF

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O1	Pd 0--1	0.63	2.49	1.23	6.45
	Pd 1--0	0.21	2.00	0.92	5.85
	Tr 0--1	2.22	6.02	5.25	11.80
	Tf 1--0	2.21	4.86	4.68	10.43
B2---O1	Pd 0--1	N/A	N/A	N/A	N/A
	Pd 1--0	N/A	N/A	N/A	N/A
	Tr 0--1	N/A	N/A	N/A	N/A
	Tf 1--0	N/A	N/A	N/A	N/A
A1---O2	Pd 0--1	N/A	N/A	N/A	N/A
	Pd 1--0	N/A	N/A	N/A	N/A
	Tr 0--1	N/A	N/A	N/A	N/A
	Tf 1--0	N/A	N/A	N/A	N/A
B2---O2	Pd 0--1	0.63	2.49	1.23	6.45
	Pd 1--0	0.21	2.00	0.92	5.85
	Tr 0--1	2.22	6.02	5.25	11.80
	Tf 1--0	2.21	4.86	4.68	10.43

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	13	2
51	13	2
20	29	2
21	29	2

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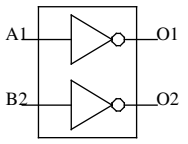
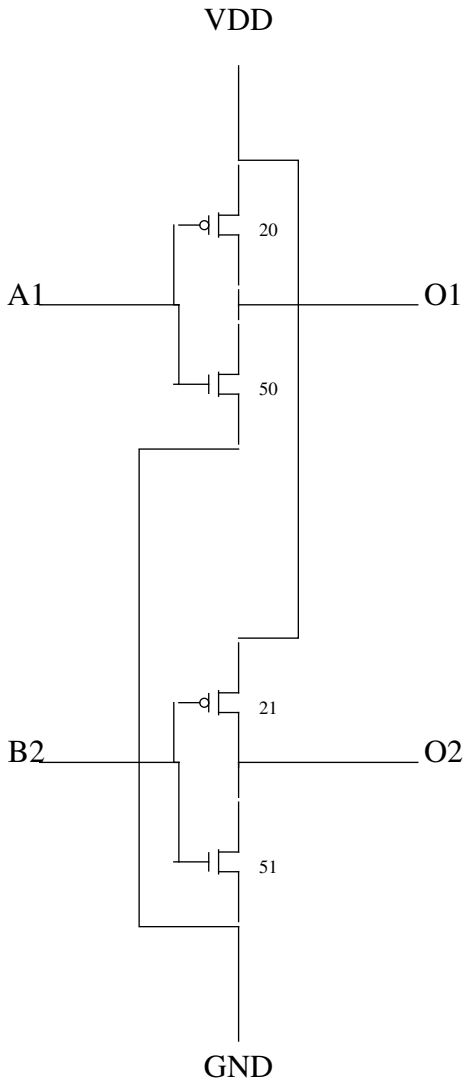
SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**invf201** DUAL_INVERTER	DATE: Mar 5,1990 VERSION: dlmV2.2



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	O1	31	0
2	A1	30	1
3	B2	30	2
4	O2	31	0

LOGIC EQUATIONS: O1 = A'
O2 = B'

Truth Table

A	B	O1	O2
0	-	1	0
-	0	0	1