********** SPICE DECK **********

*** Generated from labf111.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 628905226
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale = 1000 units

M12x39 21 23 vdd vdd PMOS W=31.0U L=2.0U
M20x39 21 22 vdd vdd PMOS W=31.0U L=2.0U
M28x39 22 21 vdd vdd PMOS W=31.0U L=2.0U
M36x39 22 20 vdd vdd PMOS W=31.0U L=2.0U
M16x4 21 23 150 gnd NMOS W=20.0U L=2.0U
M20x4 150 22 gnd gnd NMOS W=20.0U L=2.0U
M28x4 151 21 gnd gnd NMOS W=20.0U L=2.0U
M32x4 151 20 22 gnd NMOS W=20.0U L=2.0U
C1 23 gnd 7.85fF
C2 22 gnd 103.81fF
C3 21 gnd 103.91fF
C4 20 gnd 7.85fF
C6 150 gnd 11.79fF
C7 151 gnd 11.79fF

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
SET2---Q	Pd 0--1	1.12	2.88	2.79	6.75
	Pd 1--0	0.56	2.83	1.93	6.44
	Tr 0--1	2.85	6.22	6.35	12.04
	Tf 1--0	2.96	6.41	6.24	12.21
RST1---Q	Pd 0--1	1.12	2.88	2.56	6.75
	Pd 1--0	1.41	4.48	3.15	10.96
	Tr 0--1	2.68	6.09	6.31	11.72
	Tf 1--0	1.31	5.81	2.53	9.94
SET2---Q_B	Pd 0--1	1.12	2.88	2.57	6.75
	Pd 1--0	1.41	4.48	3.15	10.96
	Tr 0--1	2.68	6.09	6.31	11.72
	Tf 1--0	1.31	5.81	2.53	9.94
RST1---Q_B	Pd 0--1	1.12	2.88	2.79	6.75
	Pd 1--0	0.56	2.84	1.93	6.44
	Tr 0--1	2.85	6.22	6.35	12.04
	Tf 1--0	2.96	6.41	6.24	12.21

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	20	2
51	20	2
52	20	2
53	20	2
22	31	2
21	31	2
20	31	2
23	31	2

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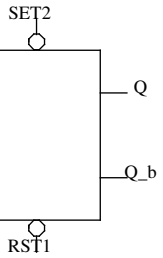
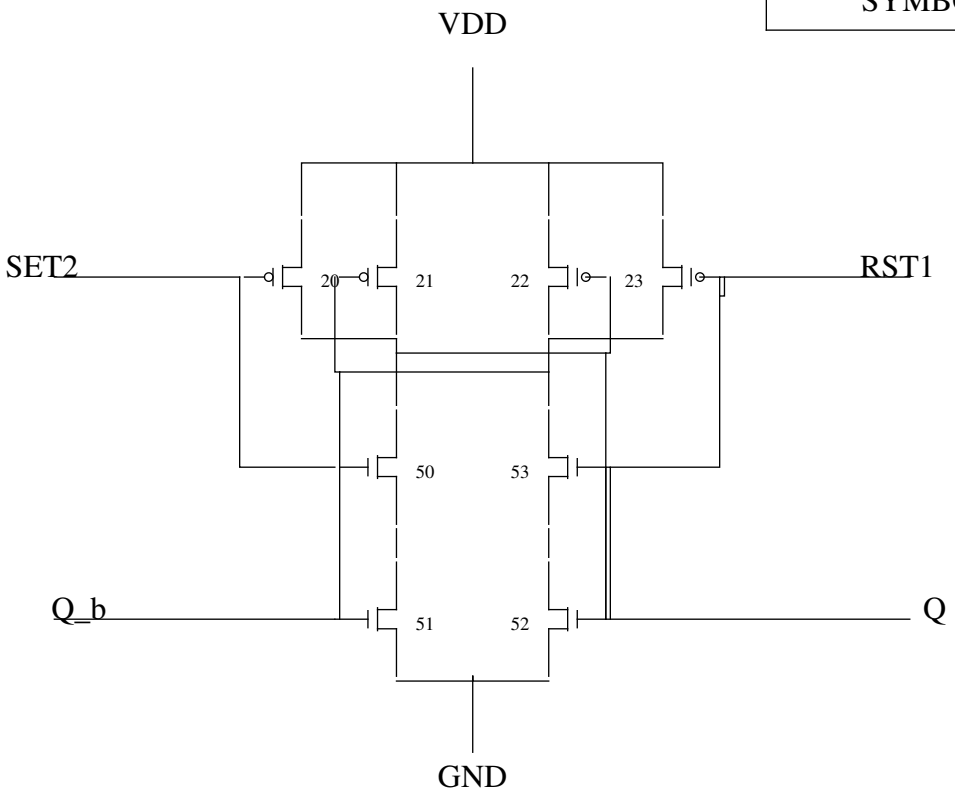
ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**labf111** NAND_LATCH	DATE: Mar 4,1990 VERSION: dlmV2.2



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	RST1	33	2
2	Q_b	26	0
3	FeedThru	----	----
4	FeedThru	----	----
5	Q	26	0
6	SET2	33	1

LOGIC EQUATIONS: Q = (Qn-1 * S * R) + S'
Q' = (Qn-1' * S * R) + R'

Truth Table

S	R	Q	Q'
0	0	1	1
0	1	1	0
1	0	0	1
1	1	Qn-1	Qn-1'
0	-	1	-
-	0	-	1