********** SPICE DECK **********

*** Generated from labf211.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 628905226
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale = 1000 units

M16x33 23 20 120 vdd PMOS W=37.0U L=2.0U
M20x33 120 21 vdd vdd PMOS W=37.0U L=2.0U
M28x33 121 23 vdd vdd PMOS W=37.0U L=2.0U
M32x33 121 22 21 vdd PMOS W=37.0U L=2.0U
M8x4 23 20 gnd gnd NMOS W=12.0U L=2.0U
M16x4 23 21 gnd gnd NMOS W=12.0U L=2.0U
M32x4 21 23 gnd gnd NMOS W=12.0U L=2.0U
M40x4 21 22 gnd gnd NMOS W=12.0U L=2.0U
C1 20 gnd 9.79fF
C2 21 gnd 110.33fF
C3 23 gnd 110.51fF
C4 22 gnd 9.79fF
C6 120 gnd 21.59fF
C7 121 gnd 21.59fF

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
SET2---Q	Pd 0--1	1.30	5.33	3.42	12.67
	Pd 1--0	0.71	2.63	2.15	6.73
	Tr 0--1	1.79	8.06	3.55	13.92
	Tf 1--0	2.92	5.53	6.24	10.91
RST1---Q	Pd 0--1	1.18	4.11	2.78	8.47
	Pd 1--0	0.71	2.63	2.15	6.77
	Tr 0--1	3.64	8.35	7.04	15.89
	Tf 1--0	2.92	5.53	6.24	11.49
SET2---Q_B	Pd 0--1	1.12	4.11	2.78	8.47
	Pd 1--0	0.71	2.63	2.15	6.73
	Tr 0--1	3.45	8.35	7.04	15.89
	Tf 1--0	2.92	5.55	6.23	10.98
RST1---Q_B	Pd 0--1	1.30	5.33	3.42	12.67
	Pd 1--0	0.71	2.63	2.15	6.73
	Tr 0--1	1.79	8.06	3.55	13.92
	Tf 1--0	2.92	5.55	6.23	10.91

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	12	2
51	12	2
52	12	2
53	12	2
21	37	2
20	37	2
22	37	2
23	37	2

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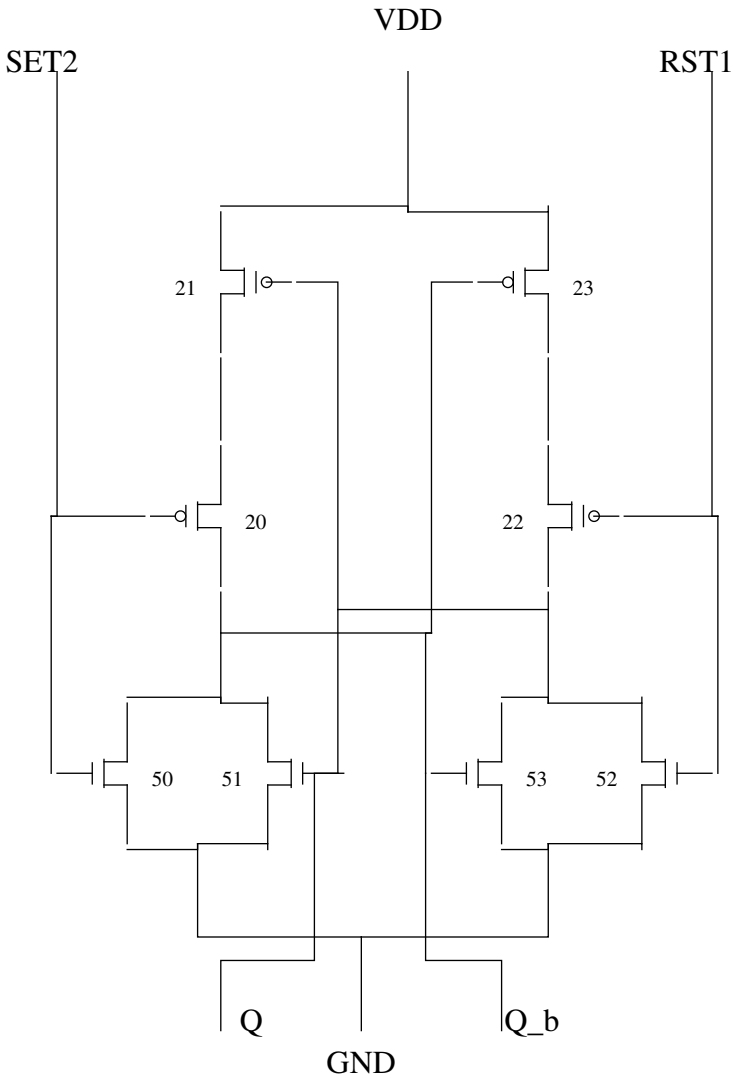
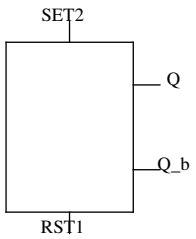
ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**labf211** NOR_LATCH	DATE: Mar 4,1990 VERSION: dlmV2.2





SYMBOL

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SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**labf211** NOR_LATCH	DATE: Mar 4,1990 VERSION: dlmV2.2

TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	SET2	33	1
2	Q_b	25	0
3	FeedThru	----	----
4	FeedThru	----	----
5	Q	25	0
6	RST1	33	2

LOGIC EQUATIONS: Q = (S * R)+(Qn-1*S'*R')
Q' = (S' * R)+(Qn-1' * S' * R')

Truth Table

S	R	Q	Q'
0	0	Qn-1	Qn-1'
0	1	0	1
1	0	1	0
1	1	0	0
1	-	-	0
-	1	0	-