********** SPICE DECK CONTINUED **********

C6 50 gnd 7.25fF
C7 Q gnd 101.81fF
C8 53 gnd 97.52fF
C9 DATA1 gnd 7.03fF
C10 57 gnd 66.86fF
C11 120 gnd 14.03fF
C12 150 gnd 6.64fF
C13 151 gnd 13.11fF

********** SPICE DECK **********

*** Generated from larf310.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 636652728
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale = 1000 units

M8x41 51 50 vdd vdd PMOS W=21.0U L=2.0U
M16x41 53 51 vdd vdd PMOS W=21.0U L=2.0U
M32x43 57 DATA1 vdd vdd PMOS W=19.0U L=2.0U
M40x39 120 57 vdd vdd PMOS W=23.0U L=2.0U
M44x39 120 53 26 vdd PMOS W=23.0U L=2.0U
M52x39 26 51 Q vdd PMOS W=30.0U L=2.0U
M60x39 Q Q_b vdd vdd PMOS W=31.0U L=2.0U
M68x39 Q_b 26 vdd vdd PMOS W=31.0U L=2.0U
M76x39 Q_b 25 vdd vdd PMOS W=31.0U L=2.0U
M8x12 51 50 gnd gnd NMOS W=11.0U L=2.0U
M16x12 53 51 gnd gnd NMOS W=11.0U L=2.0U
M32x15 57 DATA1 gnd gnd NMOS W=10.0U L=2.0U
M40x15 150 57 gnd gnd NMOS W=10.0U L=2.0U
M44x15 150 51 26 gnd NMOS W=10.0U L=2.0U
M52x13 26 53 Q gnd NMOS W=16.0U L=2.0U
M60x4 Q Q_b gnd gnd NMOS W=25.0U L=2.0U
M76x4 151 26 gnd gnd NMOS W=23.0U L=2.0U
M80x4 151 25 Q_b gnd NMOS W=23.0U L=2.0U
C1 51 gnd 89.67fF
C2 Q_b gnd 103.61fF
C3 26 gnd 90.44fF
C4 25 gnd 7.14fF

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
CLK2---Q	Pd 0--1	3.31	6.86	7.14	13.97
	Pd 1--0	1.41	4.34	3.43	10.54
	Tr 0--1	0.70	4.58	1.44	8.89
	Tf 1--0	1.38	3.64	2.67	6.84
DATA1---Q	Pd 0--1	2.08	5.50	4.89	11.60
	Pd 1--0	2.46	5.06	5.99	11.58
	Tr 0--1	0.99	5.45	1.77	9.28
	Tf 1--0	0.70	3.14	1.25	5.97
RST3---Q	Pd 0--1	N/A	N/A	N/A	N/A
	Pd 1--0	1.41	4.34	3.43	10.54
	Tr 0--1	N/A	N/A	N/A	N/A
	Tf 1--0	1.38	3.64	2.67	6.84
CLK2---Q_B	Pd 0--1	1.19	2.97	2.76	7.11
	Pd 1--0	2.89	4.34	6.37	9.01
	Tr 0--1	2.41	5.21	5.61	11.19
	Tf 1--0	1.23	4.18	2.47	7.68
DATA1---Q_B	Pd 0--1	2.36	3.86	5.65	8.54
	Pd 1--0	1.66	2.94	4.12	6.59
	Tr 0--1	1.60	5.11	2.97	9.00
	Tf 1--0	1.54	4.77	3.06	7.44
RST3---Q_B	Pd 0--1	1.19	2.97	2.76	7.11
	Pd 1--0	N/A	N/A	N/A	N/A
	Tr 0--1	2.41	5.21	5.61	11.19
	Tf 1--0	N/A	N/A	N/A	N/A

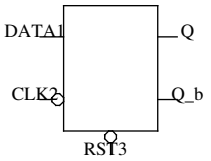
Cell Device Sizes

Transistor	Width (λ)	Length (λ)
58	10	2
54	25	2
56	23	2
55	23	2
57	10	2
52	10	2
53	16	2
50	11	2
51	11	2
28	19	2
20	21	2
21	21	2
24	31	2
23	30	2
22	23	2
27	23	2
26	31	2
25	31	2

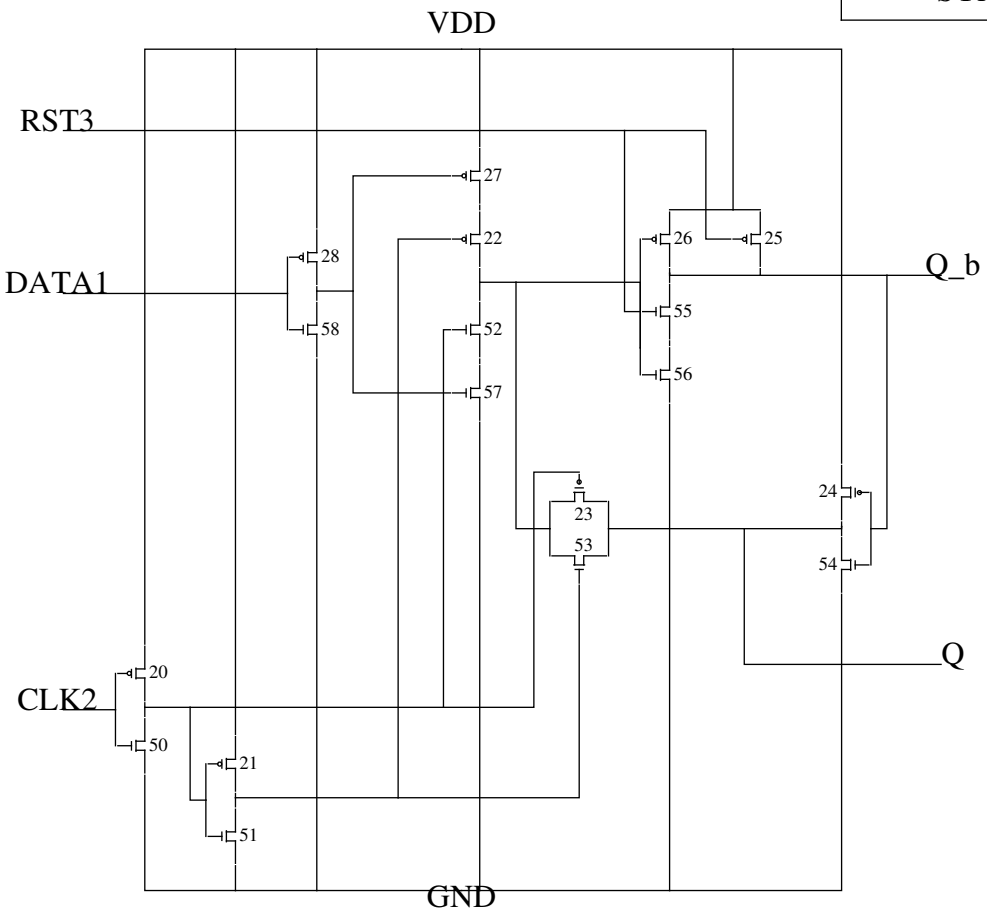
Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**larf310** CLOCKED_LATCH_W/RST	DATE: Mar 6,1990 VERSION: dlmV2.2



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	FeedThru	----	----
2	CLK2	25	1
3	FeedThru	----	----
4	DATA1	39	3
5	FeedThru	----	----
6	FeedThru	----	----
7	Q	33	0
8	Blocked		----
9	FeedThru	----	----
10	Q_b	32	0
11	RST3	36	2

LOGIC EQUATIONS: Q = [(Qn-1 * C) + (D * C')]*R
Q' = (NOT Q)

Truth Table

C	D	R	Q	Q'
h2l	-	1	D	D'
l2h	-	1	Qn-1	Qn-1'
1	-	1	Qn-1	Qn-1'
0	0	1	0	1
0	1	1	1	0
-	-	0	0	1