********** SPICE DECK **********

*** Generated from muxf201.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 634234332
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale = 1000 units

M8x39 O 20 vdd vdd PMOS W=23.0U L=2.0U
M16x43 120 21 vdd vdd PMOS W=27.0U L=2.0U
M20x43 120 22 20 vdd PMOS W=27.0U L=2.0U
M28x43 20 23 121 vdd PMOS W=27.0U L=2.0U
M32x43 121 25 vdd vdd PMOS W=27.0U L=2.0U
M40x43 22 25 vdd vdd PMOS W=19.0U L=2.0U
M8x12 O 20 gnd gnd NMOS W=14.0U L=2.0U
M16x12 150 21 gnd gnd NMOS W=11.0U L=2.0U
M20x12 150 25 20 gnd NMOS W=11.0U L=2.0U
M28x12 20 23 151 gnd NMOS W=11.0U L=2.0U
M32x12 151 22 gnd gnd NMOS W=11.0U L=2.0U
M40x12 22 25 gnd gnd NMOS W=11.0U L=2.0U
C1 21 gnd 7.77fF
C2 22 gnd 70.93fF
C3 23 gnd 8.58fF
C4 25 gnd 21.48fF
C6 20 gnd 78.09fF
C7 O gnd 74.33fF
C8 120 gnd 16.19fF
C9 121 gnd 16.19fF
C10 150 gnd 7.08fF
C11 151 gnd 7.08fF

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	1.42	3.40	4.20	8.26
	Pd 1--0	1.54	2.61	3.20	6.46
	Tr 0--1	1.37	6.02	2.78	10.62
	Tf 1--0	1.39	4.30	2.79	7.43
B2---O	Pd 0--1	1.36	3.34	4.20	8.26
	Pd 1--0	1.42	2.38	3.43	6.06
	Tr 0--1	2.31	6.06	2.90	10.51
	Tf 1--0	1.19	4.29	2.00	7.04
SEL3---O	Pd 0--1	2.15	4.27	4.75	8.50
	Pd 1--0	1.21	2.64	3.17	6.23
	Tr 0--1	1.26	6.23	2.53	10.62
	Tf 1--0	1.17	3.97	1.93	6.30

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	14	2
51	11	2
53	11	2
52	11	2
54	11	2
55	11	2
20	23	2
21	27	2
22	27	2
23	27	2
24	27	2
25	19	2

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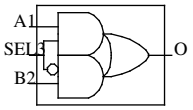
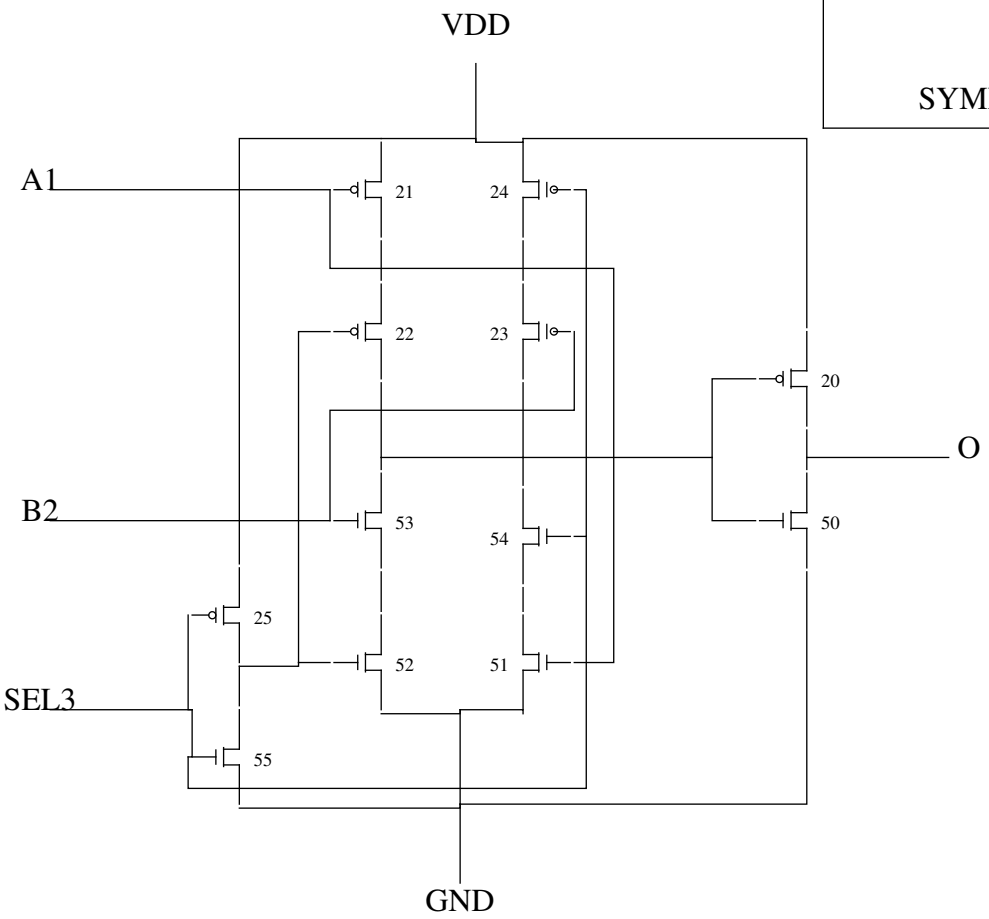
SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**muxf201** DATA_SELECT	DATE: Mar 3,1990 VERSION: dlmV2.2



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	O	35	0
2	FeedThru	----	----
3	A1	27	1
4	B2	30	2
5	FeedThru	----	----
6	SEL3	31	3

LOGIC EQUATIONS: O = (A * SEL) + (B * SEL')

Truth Table

A	SEL	B	O
-	0	1	1
1	1	-	1