********** SPICE DECK **********

*** Generated from nanf201.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 628905226
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale = 1000 units

M8x45 O 20 vdd vdd PMOS W=25.0U L=2.0U
M16x45 O 21 vdd vdd PMOS W=25.0U L=2.0U
M12x4 150 20 gnd gnd NMOS W=21.0U L=2.0U
M16x4 150 21 O gnd NMOS W=21.0U L=2.0U
C1 20 gnd 9.75fF
C2 21 gnd 8.29fF
C4 O gnd 83.27fF
C5 150 gnd 12.23fF

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1---O	Pd 0--1	1.13	3.09	2.98	7.75
	Pd 1--0	0.93	2.50	2.72	7.34
	Tr 0--1	2.85	6.57	5.92	12.77
	Tf 1--0	3.03	5.51	5.59	11.37

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
51	21	2
50	21	2
21	25	2
20	25	2

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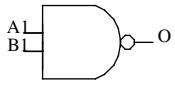
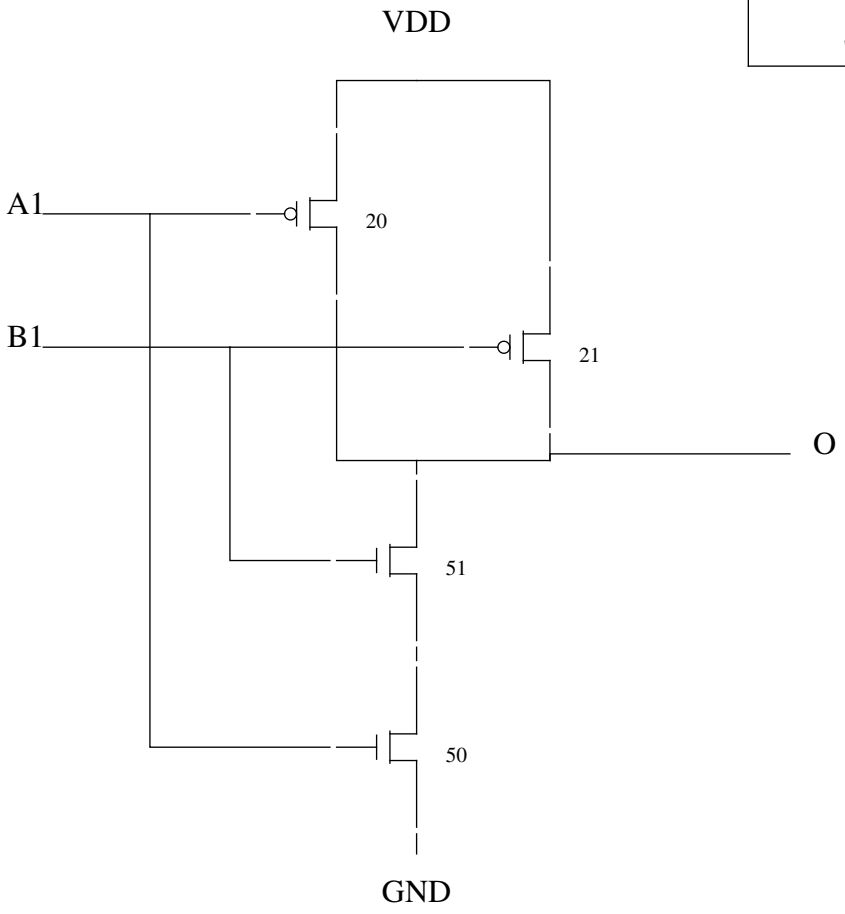
SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**nanf201** 2_INPUT_NAND	DATE: Mar 4,1990 VERSION: dlmV2.2



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	A1	27	1
2	O	39	0
3	B1	27	1

LOGIC EQUATIONS: O = (A * B)'

Truth Table

A	B	O
0	-	1
-	0	1