********** SPICE DECK **********

*** Generated from nanf211.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 628905226
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale = 1000 units

M8x47 O1 21 vdd vdd PMOS W=23.0U L=2.0U
M16x47 O1 20 vdd vdd PMOS W=23.0U L=2.0U
M24x44 O2 O1 vdd vdd PMOS W=26.0U L=2.0U
M8x4 O1 21 150 gnd NMOS W=21.0U L=2.0U
M12x4 150 20 gnd gnd NMOS W=21.0U L=2.0U
M24x12 O2 O1 gnd gnd NMOS W=14.0U L=2.0U
C1 21 gnd 9.84fF
C2 20 gnd 9.66fF
C3 O1 gnd 90.01fF
C5 O2 gnd 79.49fF
C6 150 gnd 12.23fF

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1---O1	Pd 0--1	1.56	3.41	3.93	8.52
	Pd 1--0	1.01	2.56	3.16	7.49
	Tr 0--1	3.06	7.32	6.49	13.91
	Tf 1--0	3.00	5.68	6.06	11.86
A1,B1---O2	Pd 0--1	1.40	5.21	3.86	12.78
	Pd 1--0	1.75	5.36	4.45	12.95
	Tr 0--1	1.18	6.44	2.11	10.60
	Tf 1--0	1.75	5.11	2.23	8.65

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
51	21	2
50	21	2
52	14	2
22	26	2
20	23	2
21	23	2

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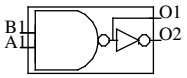
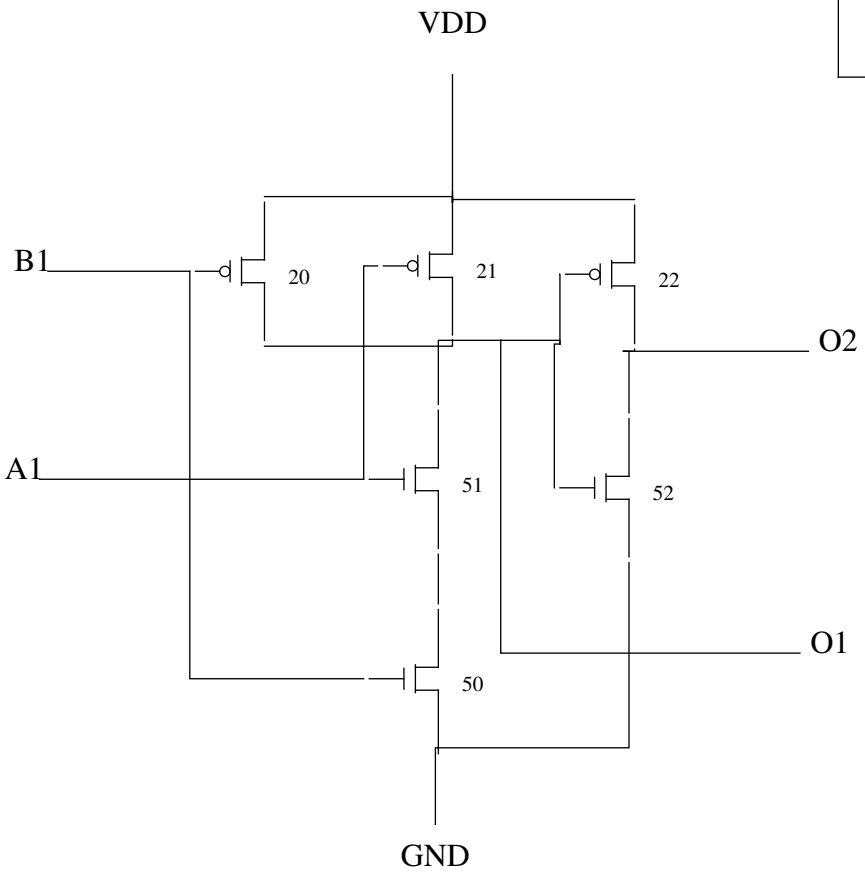
ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**nanf211** 2_INPUT_NAND/AND	DATE: Mar 3,1990 VERSION: dlmV2.2



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	A1	34	1
2	O1	43	0
3	B1	40	1
4	O2	34	0

LOGIC EQUATIONS: O1 = (A * B)'
O2 = A * B

Truth Table

A	B	O1	O2
0	-	1	0
-	0	1	0
1	1	0	1