********** SPICE DECK **********

*** Generated from nanf251.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 628905226
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale = 1000 units

M8x39 21 50 vdd vdd PMOS W=10.0U L=2.0U
M16x47 O 21 vdd vdd PMOS W=23.0U L=2.0U
M24x47 O 22 vdd vdd PMOS W=23.0U L=2.0U
M8x20 21 50 gnd gnd NMOS W=7.0U L=2.0U
M16x4 150 21 gnd gnd NMOS W=23.0U L=2.0U
M20x4 150 22 O gnd NMOS W=23.0U L=2.0U
C1 21 gnd 49.26fF
C2 22 gnd 12.92fF
C4 50 gnd 9.43fF
C5 O gnd 89.06fF
C6 150 gnd 13.11fF

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1---O	Pd 0--1	1.10	2.93	2.87	6.36
	Pd 1--0	1.79	2.90	5.20	9.05
	Tr 0--1	1.59	6.17	3.52	10.89
	Tf 1--0	1.36	4.62	2.59	7.98
B2---O	Pd 0--1	1.06	3.70	2.67	8.03
	Pd 1--0	1.70	2.90	5.20	9.05
	Tr 0--1	2.64	6.55	5.07	12.95
	Tf 1--0	2.78	5.34	5.49	11.16

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
52	23	2
51	23	2
50	7	2
20	10	2
21	23	2
22	23	2

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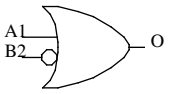
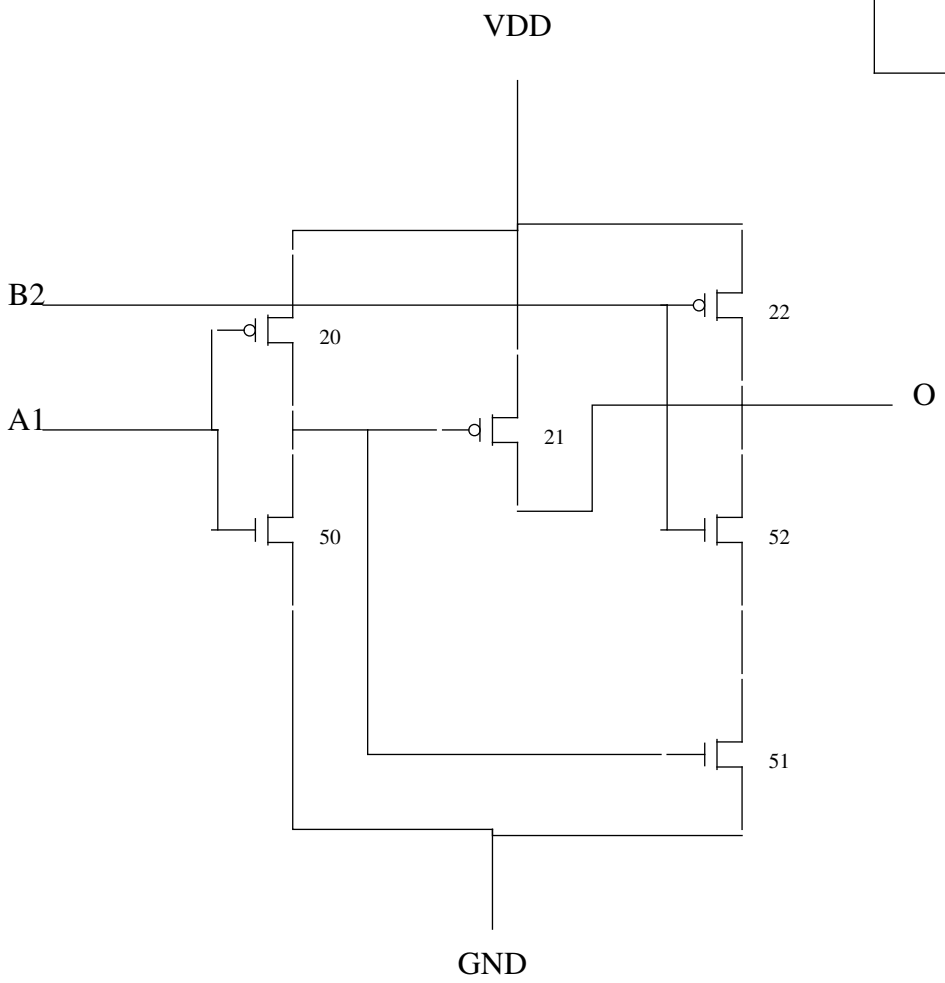
SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**nanf251** A_OR_B'	DATE: Mar 3,1990 VERSION: dlmV2.2



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	A1	56	1
2	FeedThru	----	----
3	O	52	0
4	B2	33	2

LOGIC EQUATIONS: O = A + B'

Truth Table

A	B	O
-	0	1
1	-	1