********** SPICE DECK **********

*** Generated from nanf311.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 628905226
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale = 1000 units

M8x46 O1 52 vdd vdd PMOS W=24.0U L=2.0U
M16x46 O1 51 vdd vdd PMOS W=24.0U L=2.0U
M24x46 O1 A1 vdd vdd PMOS W=24.0U L=2.0U
M40x45 O2 O1 vdd vdd PMOS W=25.0U L=2.0U
M20x4 O1 52 150 gnd NMOS W=23.0U L=2.0U
M24x4 150 51 151 gnd NMOS W=23.0U L=2.0U
M28x4 151 A1 gnd gnd NMOS W=23.0U L=2.0U
M36x12 O2 O1 gnd gnd NMOS W=15.0U L=2.0U
C1 52 gnd 10.10fF
C2 51 gnd 8.99fF
C3 A1 gnd 8.99fF
C4 O1 gnd 141.78fF
C6 O2 gnd 76.18fF
C7 150 gnd 13.11fF
C8 151 gnd 13.11fF

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1,C1---O1	Pd 0--1	1.86	3.49	4.46	8.66
	Pd 1--0	1.72	3.51	5.60	10.44
	Tr 0--1	3.53	7.60	7.76	14.41
	Tf 1--0	3.42	7.11	7.00	14.34
A1,B1,C1---O2	Pd 0--1	2.13	6.55	6.37	16.54
	Pd 1--0	1.99	5.30	4.94	12.84
	Tr 0--1	1.37	6.77	2.56	11.27
	Tf 1--0	2.53	5.04	2.34	8.36

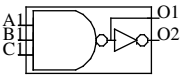
Cell Device Sizes

Transistor	Width (λ)	Length (λ)
53	15	2
50	23	2
51	23	2
52	23	2
20	24	2
23	25	2
22	24	2
21	24	2

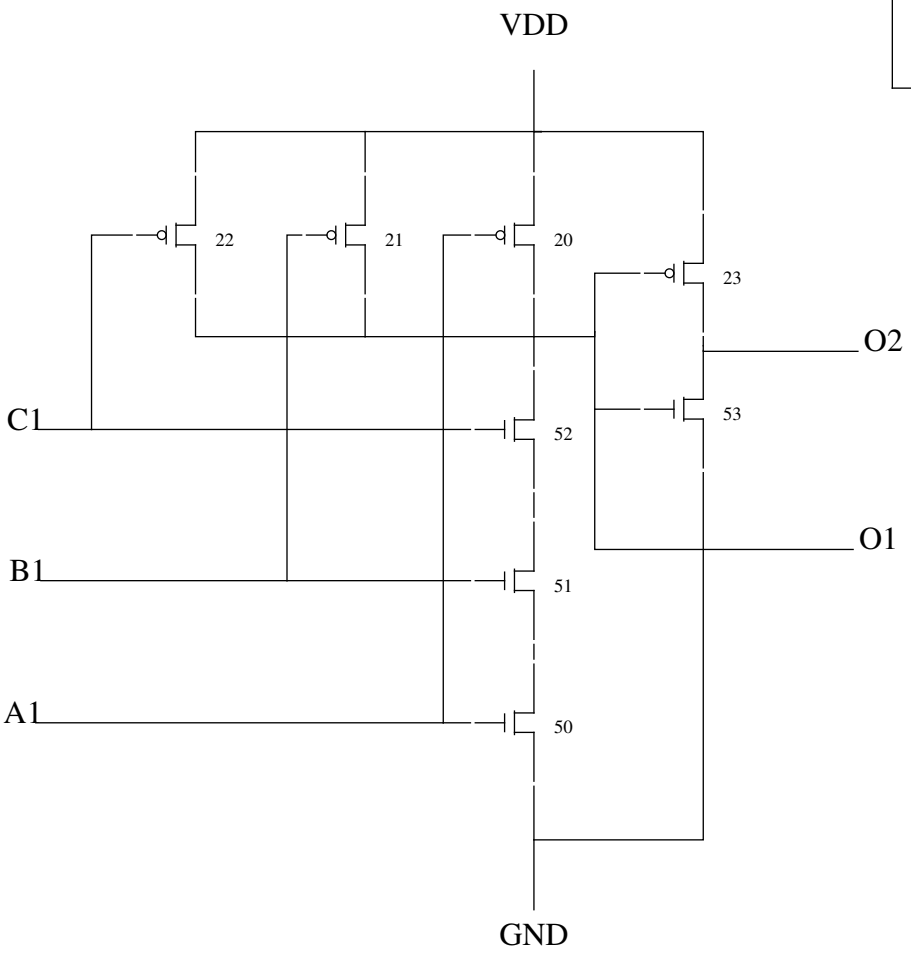
Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**nanf311** 3_INPUT_NAND/AND	DATE: Mar 3,1990 VERSION: dlmV2.2



SYMBOL



Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**nanf311** 3_INPUT_NAND/AND	DATE: Mar 3,1990 VERSION: dlmV2.2

TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	FeedThru	----	----
2	C1	41	1
3	B1	41	1
4	A1	41	1
5	O1	41	0
6	O2	41	0

LOGIC EQUATIONS: O1 = (A * B * C)'
O2 = A * B * C

Truth Table

A	B	C	O1	O2
0	-	-	1	0
-	0	-	1	0
-	-	0	1	0
1	1	1	0	1