********** SPICE DECK **********

*** Generated from nanf401.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 628905226
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale = 1000 units

M8x48 O D1 vdd vdd PMOS W=22.0U L=2.0U
M16x48 O 52 vdd vdd PMOS W=22.0U L=2.0U
M24x48 O B1 vdd vdd PMOS W=22.0U L=2.0U
M32x48 O 50 vdd vdd PMOS W=22.0U L=2.0U
M16x4 O D1 150 gnd NMOS W=24.0U L=2.0U
M20x4 150 52 151 gnd NMOS W=24.0U L=2.0U
M24x4 151 B1 152 gnd NMOS W=24.0U L=2.0U
M28x4 152 50 gnd gnd NMOS W=24.0U L=2.0U
C1 O vdd 5.36fF
C2 D1 gnd 10.00fF
C3 52 gnd 7.99fF
C4 B1 gnd 7.53fF
C5 50 gnd 8.48fF
C7 O gnd 134.42fF
C8 150 gnd 13.55fF
C9 151 gnd 13.55fF
C10 152 gnd 13.55fF

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1,C1,D1---O	Pd 0--1	1.77	3.67	4.35	9.04
	Pd 1--0	2.01	4.18	6.09	12.04
	Tr 0--1	3.76	7.89	8.30	15.06
	Tf 1--0	3.83	8.19	7.06	16.10

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
53	24	2
52	24	2
51	24	2
50	24	2
23	22	2
22	22	2
21	22	2
20	22	2

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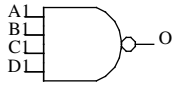
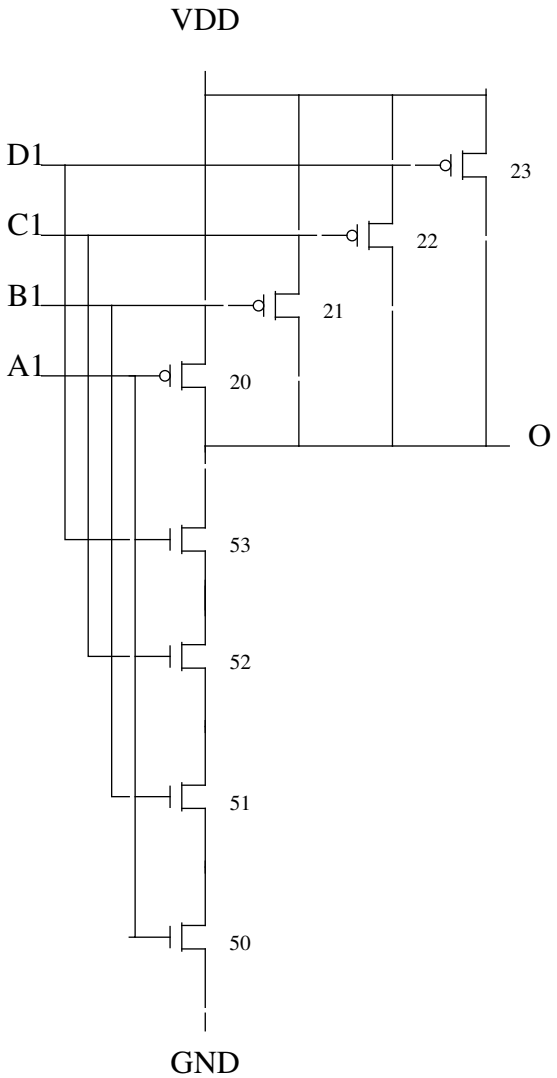
SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**nanf401** 4_INPUT_NAND	DATE: Mar 3,1990 VERSION: dlmV2.2



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	D1	35	1
2	O	42	0
3	C1	42	1
4	B1	40	1
5	A1	35	1

LOGIC EQUATIONS: O = (A * B * C * D)'

Truth Table

A	B	C	D	O
0	-	-	-	1
-	0	-	-	1
-	-	0	-	1
-	-	-	0	1