********** SPICE DECK **********

*** Generated from nanf411.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 628905226
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale = 1000 units

M8x53 54 D1 vdd vdd PMOS W=17.0U L=2.0U
M16x53 54 C1 vdd vdd PMOS W=17.0U L=2.0U
M24x53 54 B1 vdd vdd PMOS W=17.0U L=2.0U
M32x53 54 A1 vdd vdd PMOS W=17.0U L=2.0U
M40x47 O2 54 vdd vdd PMOS W=23.0U L=2.0U
M12x4 54 D1 150 gnd NMOS W=25.0U L=2.0U
M16x4 150 C1 151 gnd NMOS W=25.0U L=2.0U
M20x4 151 B1 152 gnd NMOS W=25.0U L=2.0U
M24x4 152 A1 gnd gnd NMOS W=25.0U L=2.0U
M40x4 O2 54 gnd gnd NMOS W=17.0U L=2.0U
C1 D1 gnd 10.16fF
C2 C1 gnd 8.82fF
C3 B1 gnd 9.46fF
C4 A1 gnd 10.12fF
C5 54 gnd 126.96fF
C7 O2 gnd 74.76fF
C8 150 gnd 13.99fF
C9 151 gnd 13.99fF
C10 152 gnd 13.99fF

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1,C1,D1---O1	Pd 0--1	2.49	4.70	6.03	11.04
	Pd 1--0	1.95	4.04	6.09	11.61
	Tr 0--1	4.12	9.59	8.87	18.24
	Tf 1--0	3.69	8.22	7.50	16.38
A1,B1,C1,D1---O2	Pd 0--1	2.47	7.62	7.11	18.54
	Pd 1--0	2.49	6.29	6.29	15.16
	Tr 0--1	1.64	7.34	2.89	12.39
	Tf 1--0	1.42	5.22	2.68	8.66

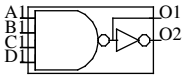
Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	25	2
51	25	2
52	25	2
53	25	2
54	17	2
23	17	2
22	17	2
21	17	2
20	17	2
24	23	2

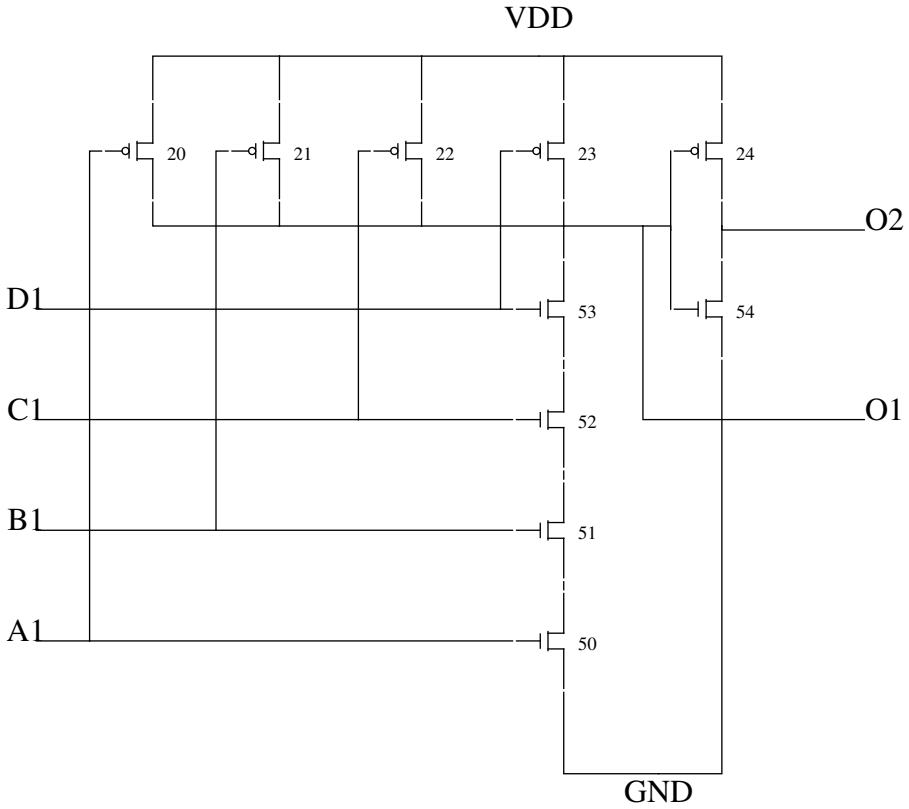
Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**nanf411** 4_INPUT_NAND/AND	DATE: Mar 3,1990 VERSION: dlmV2.2



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	D1	27	1
2	C1	42	1
3	O1	48	0
4	B1	42	1
5	A1	33	1
6	O2	34	0

LOGIC EQUATIONS: O1 = (A * B * C * D)'
O2 = A * B * C * D

Truth Table

A	B	C	D	O1	O2
0	-	-	-	1	0
-	0	-	-	1	0
-	-	0	-	1	0
-	-	-	0	1	0
1	1	1	1	0	1