********** SPICE DECK **********

*** Generated from oaif2201.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 628905226
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale = 1000 units

M12x44 120 50 vdd vdd PMOS W=26.0U L=2.0U
M16x44 120 51 O vdd PMOS W=26.0U L=2.0U
M24x44 O C2 121 vdd PMOS W=26.0U L=2.0U
M28x44 121 53 vdd vdd PMOS W=26.0U L=2.0U
M8x12 150 50 gnd gnd NMOS W=13.0U L=2.0U
M16x12 150 51 gnd gnd NMOS W=13.0U L=2.0U
M24x12 150 C2 O gnd NMOS W=13.0U L=2.0U
M32x12 O 53 150 gnd NMOS W=13.0U L=2.0U
C1 50 gnd 8.71fF
C2 51 gnd 7.53fF
C3 C2 gnd 7.63fF
C4 53 gnd 8.93fF
C6 120 gnd 15.65fF
C7 O gnd 74.59fF
C8 121 gnd 15.65fF
C9 150 gnd 80.32fF

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1---O	Pd 0--1	1.73	4.83	4.10	11.03
	Pd 1--0	1.68	4.44	4.92	10.95
	Tr 0--1	4.31	11.09	8.60	21.09
	Tf 1--0	3.38	7.71	7.06	14.90
C2,D2---O	Pd 0--1	1.71	4.82	3.96	11.03
	Pd 1--0	1.68	4.44	4.92	10.95
	Tr 0--1	4.31	11.09	8.24	21.09
	Tf 1--0	3.30	7.71	6.96	14.88

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
51	13	2
50	13	2
20	26	2
21	26	2
23	26	2
22	26	2

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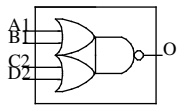
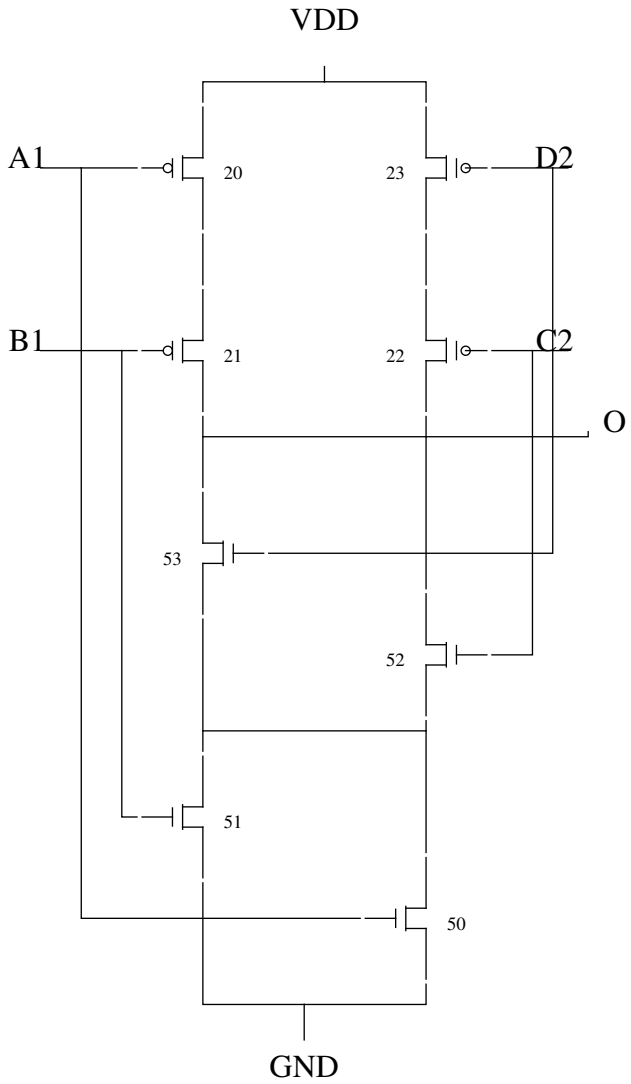
SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**oaif2201** 2/2_OR/NAND_MUX	DATE: Mar 3,1990 VERSION: dlmV2.2



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	A1	27	1
2	B1	30	1
3	C2	28	2
4	O	27	0
5	D2	32	2

LOGIC EQUATIONS: O = ((A+B) * (C+D))'

Truth Table

A	B	C	D	O
0	0	-	-	1
-	-	0	0	1