********** SPICE DECK **********

*** Generated from swcf020.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 632435398
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale = 1000 units

M8x49 20 51 vdd vdd PMOS W=21.0U L=2.0U
M24x40 DATA1 20 O vdd PMOS W=22.0U L=2.0U
M8x4 20 51 gnd gnd NMOS W=16.0U L=2.0U
M24x12 DATA1 51 O gnd NMOS W=16.0U L=2.0U
C1 51 gnd 21.67fF
C3 20 gnd 106.15fF
C4 DATA1 gnd 76.02fF
C5 O gnd 77.73fF

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
DATA1---O	Pd 0--1	0.13	1.21	0.27	2.66
	Pd 1--0	0.12	1.22	0.28	2.94
	Tr 0--1	6.12	8.41	18.18	20.85
	Tf 1--0	5.99	6.24	17.86	17.44
CTL2---O	Pd 0--1	0.00	1.58	0.79	3.88
	Pd 1--0	0.00	1.15	0.00	3.08
	Tr 0--1	2.88	6.31	5.79	11.56
	Tf 1--0	1.77	4.56	4.07	9.55

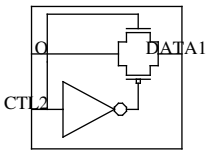
Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	16	2
51	16	2
21	21	2
20	22	2

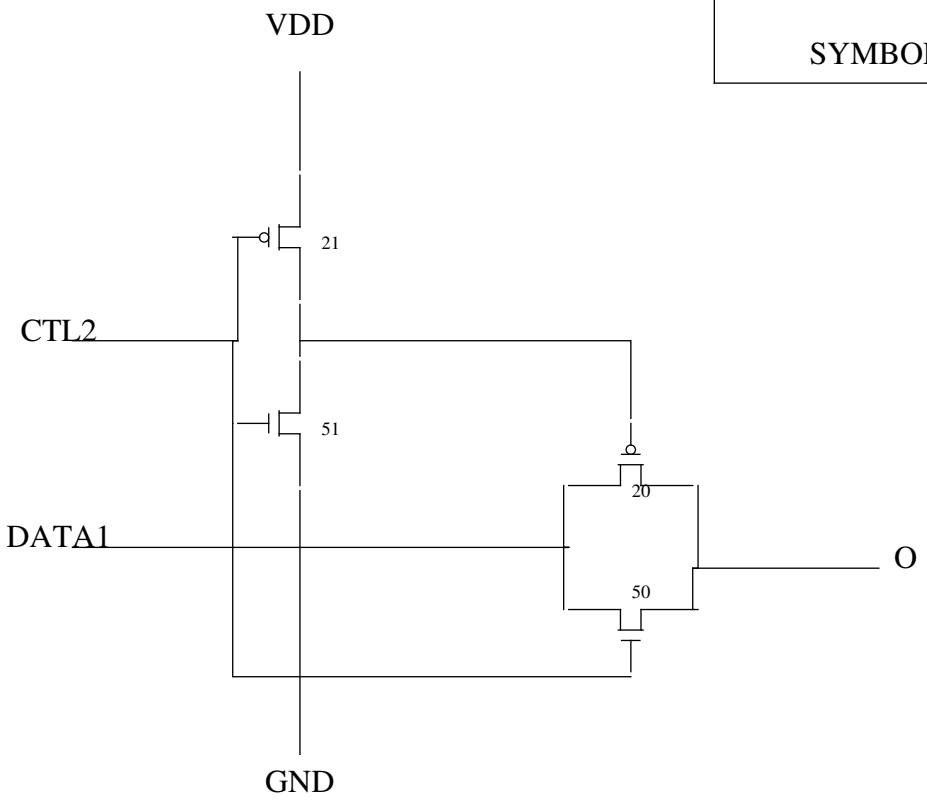
Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**swcf020** TRANSMISSION_GATE	DATE: Mar 3,1990 VERSION: dlmV2.2



SYMBOL



TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	CTL2	36	2
2	FeedThru	----	----
3	DATA1	33	1
4	O	33	0

LOGIC EQUATIONS: O = D * CTL
(Hi-Z at CTL Low)

Truth Table

CTL	D	O
1	0	0
1	1	1
1	-	-
0	0	Z
0	1	Z
0	-	Z