********** SPICE DECK **********

*** Generated from swcf120.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 622155623
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale = 1000 units

M8x49 50 CTL2 vdd vdd PMOS W=21.0U L=2.0U
M24x39 DATA1 CTL2 O vdd PMOS W=31.0U L=2.0U
M8x4 50 CTL2 gnd gnd NMOS W=16.0U L=2.0U
M24x4 DATA1 50 O gnd NMOS W=24.0U L=2.0U
C1 CTL2 gnd 14.81fF
C3 50 gnd 95.75fF
C4 DATA1 gnd 109.60fF
C5 O gnd 98.18fF

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
DATA1---O	Pd 0--1	0.11	0.84	0.24	1.83
	Pd 1--0	0.11	0.87	0.25	2.11
	Tr 0--1	6.12	7.62	18.17	19.79
	Tf 1--0	5.99	5.93	17.86	17.39
CTL2---O	Pd 0--1	0.00	1.98	0.00	4.73
	Pd 1--0	0.72	1.55	2.55	4.35
	Tr 0--1	2.26	5.83	4.88	12.17
	Tf 1--0	2.81	3.39	7.20	7.15

Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	24	2
51	16	2
21	21	2
20	31	2

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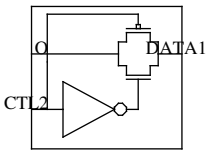
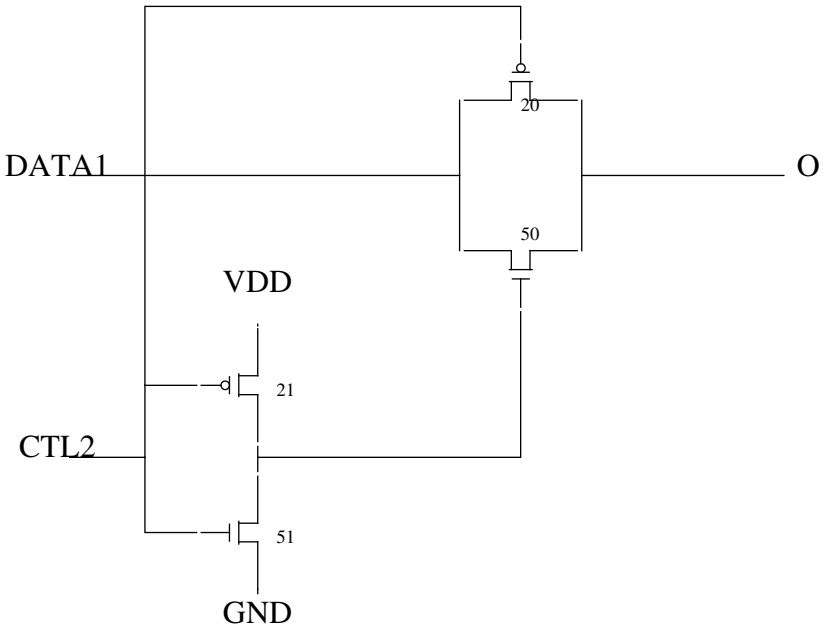
SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**swcf120** TRANSMISSION_GATE	DATE: Mar 7,1990 VERSION: dlmV2.2



SYMBOL



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TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	CTL2	31	2
2	FeedThru	----	----
3	DATA1	41	1
4	O	33	0

LOGIC EQUATIONS: O = D * CTL'
(Hi-Z at CTL High)

Truth Table

CTL	D	O
1	0	Z
1	1	Z
1	-	Z
0	0	0
0	1	1
0	-	-