********** SPICE DECK **********

*** Generated from xnof201.mag by magic's spice generator
*** technology: scmos
*** extraction style: lambda=1.0
*** units per lambda: dlm V2.20
*** timestamp: 636652825
*** version: dlm V2.2
*** Capacitance Threshold = 5000 units
*** Resistance Scale = 1000 units

M8x42 54 52 vdd vdd PMOS W=14.0U L=2.0U
M16x42 121 52 vdd vdd PMOS W=24.0U L=2.0U
M20x42 121 53 O vdd PMOS W=24.0U L=2.0U
M28x42 O 55 120 vdd PMOS W=24.0U L=2.0U
M32x42 120 54 vdd vdd PMOS W=24.0U L=2.0U
M40x42 55 53 vdd vdd PMOS W=14.0U L=2.0U
M12x23 54 52 gnd gnd NMOS W=6.0U L=2.0U
M12x5 151 52 gnd gnd NMOS W=14.0U L=2.0U
M16x5 151 55 O gnd NMOS W=14.0U L=2.0U
M28x5 O 54 150 gnd NMOS W=14.0U L=2.0U
M32x5 150 53 gnd gnd NMOS W=14.0U L=2.0U
M40x16 55 53 gnd gnd NMOS W=6.0U L=2.0U
C1 53 gnd 23.54fF
C3 52 gnd 10.13fF
C4 55 gnd 61.08fF
C5 54 gnd 53.96fF
C6 121 gnd 14.57fF
C7 O gnd 92.23fF
C8 120 gnd 14.57fF
C9 151 gnd 9.05fF
C10 150 gnd 9.05fF

2-micron delay information.

Path	Timing	Nominal Case		Worst Case	
		No Load	1pF	No Load	1pF
A1,B1---O	Pd 0--1	1.82	5.34	4.57	11.24
	Pd 1--0	1.78	4.17	4.43	7.90
	Tr 0--1	3.29	11.03	7.28	20.91
	Tf 1--0	3.29	7.15	6.91	14.06

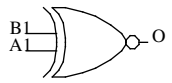
Cell Device Sizes

Transistor	Width (λ)	Length (λ)
50	6	2
51	6	2
52	14	2
53	14	2
54	14	2
55	14	2
20	14	2
21	14	2
22	24	2
23	24	2
24	24	2
25	24	2

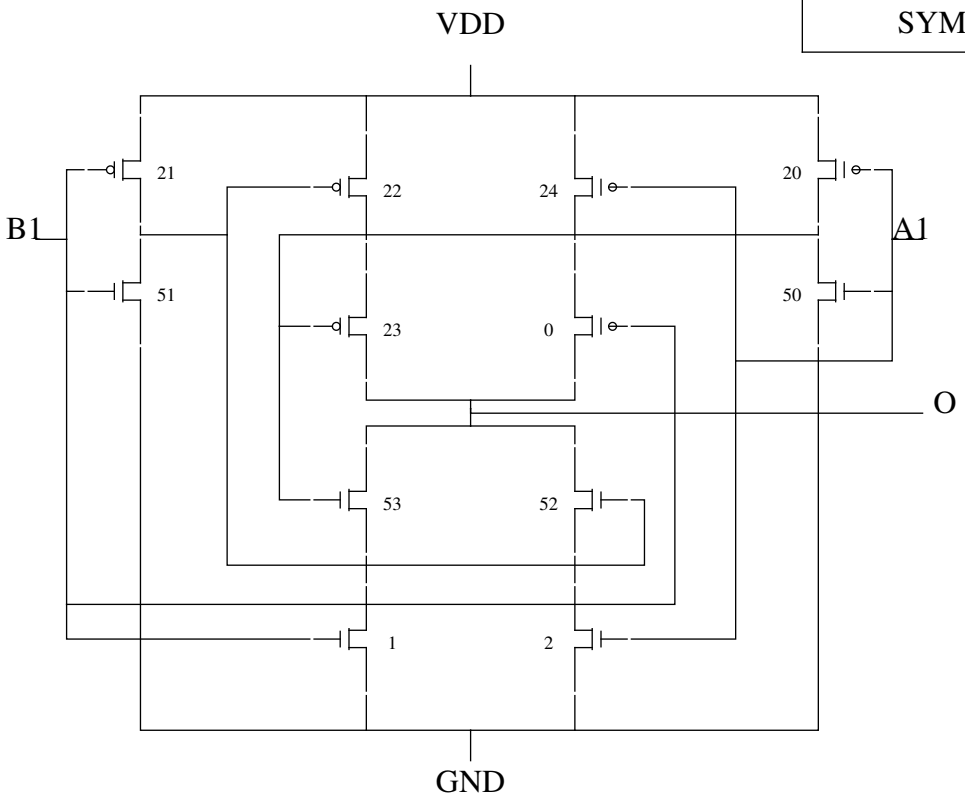
Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**xnof201** 2_INPUT_EX-NOR	DATE: Mar 6,1990 VERSION: dlmV2.2



SYMBOL



Institute for Technology Development

ADVANCED MICROELECTRONICS DIVISION

SCALABLE CMOS (SCMOS) DOUBLE METAL I / C STANDARD CELL LIBRARY	**xnof201** 2_INPUT_EX-NOR	DATE: Mar 6,1990 VERSION: dlmV2.2

TERMINAL LOCATION (In Lambda)

GRID	PIN_NAME	Y_LOC	CLASS
1	A1	33	1
2	FeedThru	----	----
3	O	56	0
4	Blocked		----
5	B1	24	1
6	FeedThru	----	----

LOGIC EQUATIONS: O = A xnor B

Truth Table

A	B	O
0	0	1
1	1	1